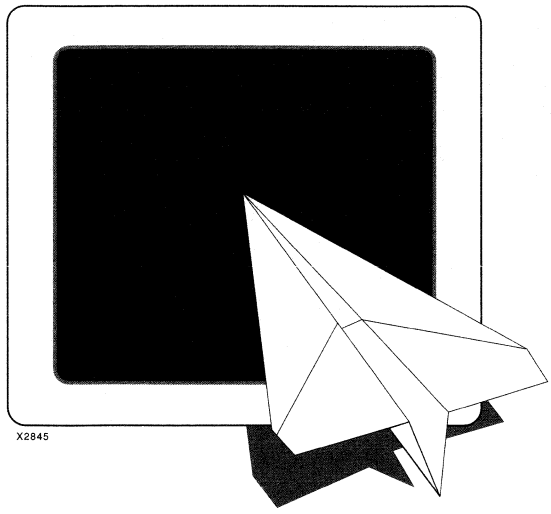



# XACT Global Index

XACT Global Index — May, 1994 (0401137 01)

Printed in U.S.A.

# Contents

Introduction ..... 1
XACT Global Index Organization ..... 1
Manuals Not Covered in the XACT Global Index ..... 2
Index ..... 3

# XACT Global Index

## Introduction

The *XACT Global Index* is being offered as a navigation tool to help the developers of Xilinx programmable-logic devices more easily locate the documentation necessary to answer questions or define specific areas of interest. Xilinx offers a wide variety of software development tools that run on different platforms. Also, demonstration boards are available to help the designer become familiar with the software, and to practice programming the devices.

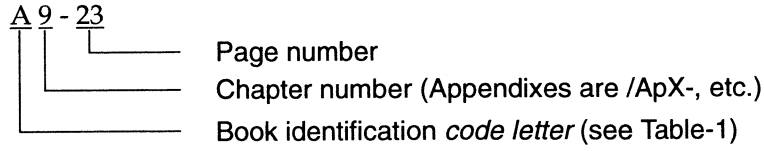
The detailed description of these tools is contained in several books or manuals. The nomenclature used to describe the operation and application of the tools is fairly consistent, but the information may be contained in more than one of the manuals. Therefore, the *XACT Global Index*, which covers most of the documents supplied by Xilinx, has been compiled. Hopefully, finding reference to most of the relevant material in one place will make it easier to find the necessary information.

Since some of the index listings are somewhat generic, the applicability is determined by the book references that are included with the accompanying page numbers. Also, it is important to check all the entry levels; first level entry (i.e., menus, profile), the second level entries (i.e., XDM, profile menu) and also third level entries (i.e., XDM, menus, profile).

## XACT Global Index Organization

The *XACT Global Index* contains the index references to all of the manuals listed in Table 1. The manuals have been assigned a *code letter* which becomes the prefix for the page numbers listed in the body of this document. This *code letter* is also defined on the top of

each page of the *XACT Global Index* for easy reference. The page number references are defined as follows.




# Manuals Not Covered in the XACT Global Index

There are six software manuals that are not indexed; *Viewlogic Workview (three volumes), ViewSynthesis* and *Xilinx-ABEL Design Reference* manuals. The *Synopsys Interface User Guide* is being revised and is not included.

The *XACT Installation Guide* should be used to get any information necessary for the installation and configuration of the software.

**Table 1 Xilinx Manuals Included in the XACT Global Index**

| Index Code Letter | Manual Title | Document ID Part Number |
|---|---|---|
| A | Xilinx ABEL User Guide | 0401136-01 |
| B | X-BLOX User Guide | 0401189-01 |
| E | XEPLD Design Guide | 0401191-01 |
| F | XEPLD Reference Guide | 0401203-01 |
| H | XACT Hardware & Peripherals Guide | 0401132-01 |
| L[a] | XACT Libraries Guide | 0401098-01 |
| M | Mentor Graphics Version 8 Interface User Guide | 0401135-01 |
| O | OrCAD Interface User Guide | 0401134-01 |
| R[b] | XACT Reference Guide, Volume I | 0401129-01 |
| | XACT Reference Guide, Volume II | 0401130-01 |
| | XACT Reference Guide, Volume III | 0401131-01 |
| U | XACT User Guide | 0401128-01 |
| V | Viewlogic Interface User Guide | 0401133-01 |

a. The "Attributes, Constraints and Carry Logic" chapter is the only one included in the *XACT Global Index*. See the *XACT Libraries Guide* for a functional Selection Guide and detailed element descriptions.

b. The *XACT Reference Guide*, Volumes I, II, and III, are identified as Chapters 1, 2 & 3 in the index page number listings.

## Symbols

":=" operator colon E2-10, E2-15
"=" operator E2-12, E2-15
$ARRAY attribute V/ApA-9
.ADD extension E5-3
.ADDMODE extension E5-3, E5-37
.bat files F5-13
.CLKF extension E3-17, E4-13
.cshrc file V11-5, V12-6, V16-6
.EXPORT extension E2-16, E5-3, E5-26
.PDS file E3-7, E4-3
.PLD file E3-7, E3-9, E4-3
.RSTF extension E2-11
.SETF extension E2-11
.SHIFT extension E5-3
.TRST extension E2-11, E2-17, E3-17, E4-13
.VST file E5-3
.WIR file E5-3
.XNF file E5-3, E5-4
@DCSET statement V14-9
@PULSEH attribute V9-5
@PULSEHI attribute V9-4
@PULSEL attribute V9-5
@PULSELO attribute V9-5, V/ApE-23
"S" parameter R2-42

## Numerics

20V8
  features supported E4-2
  using E3-4, E4-2
22V10
  features supported E4-2
  using E3-4, E4-2
3-State
  BIDIR_IO B4-18
3-State buffers O5-4
3-State control E2-11
3-State module B4-110
3-State multiplexing O5-7
3-State outputs E2-17
3-State signals A7-10, A7-12
3V Adapter H5-3
  using with XC2000L and XC3000L devices H5-12

## A

ABEL F5-15
  example files F/ApC-11
  see also PLD compilers
ABEL file
  translating F2-20
ABEL Hardware Description Language V14-1
ABEL, *see* Xilinx ABEL
ABEL-HDL M3-9, U2-3
ABEL-HDL file A1-8, V6-10, V14-3, V14-6
  @DCSET statement V14-9
  alternate directive A8-3
  async_reset keyword A4-2
  attributes A4-5, A7-13
    buffer A4-6, A7-14
    com A4-6, A7-14
    invert A4-6, A7-14, A/ApB-1
    neg A4-6, A6-11, A6-27, A7-14
    pos A4-6, A6-11, A6-27, A7-14
    reg A4-6, A7-14
    reg_d A4-6, A7-14
    reg_g A4-6, A7-14
    reg_jk A4-6, A7-14
    reg_sr A4-6, A7-14
    reg_t A4-6, A7-14
    XOR A7-14
  checking syntax A5-3, A6-11, A6-33
  combining multiple files A7-3
  comments A3-11, A3-17, A9-19, A9-20, A9-23
  compiling V14-10
  converting device-specific to device-independent design A9-33
  converting from JEDEC A7-5, A7-20, A8-1
  converting from PALASM A8-2

ABEL-HDL file *(Continued)*
converting to PLD file A5-6, A5-8, A6-10, A6-33, A6-41, A7-17, A7-18
converting to PLD format A7-19
converting to XNF file A5-5, A5-7, A6-7, A6-33
copying lines A6-4
copying text A6-22
creating options file A6-2, A6-21
DCSET directive A3-7, A9-21, A9-25
DCSTATE directive A3-7, A4-17, A6-9, A6-25
declarations statement A7-4, A9-24
deleting lines A6-4
deleting text A6-22
device statement A7-5, A7-19, A9-34, A/ApB-2
displaying parameters A6-18
dot extensions A1-11, A4-6, A4-8, A6-18, A7-2, A7-11, A7-12, A7-13
end statement A3-10, A3-13, A3-15, A3-19, A9-21, A9-25, V14-10
EPLD file structure A7-2
EPLD syntax A7-5
equations statement A3-11, A3-17, A4-17, A7-9, A9-21, V14-8
example A3-8, A3-13, A8-4, A9-18, A9-22, A9-28, A9-34
FPGA syntax A4-1
include directive A7-3, A7-4, A7-5
inserting contents of other file A6-2, A6-20
invoking non-XABEL text editor A5-3, A6-4, A6-5, A6-23
Istype keyword A7-13, A7-16, A9-24, A/ApB-2
Istype statement V14-7
module names A4-17
module statement A3-10, A3-15, A6-12, A9-19, A9-23, V14-6
moving editing window A6-22
node declarations A4-16
opening new file A6-1, A6-2, A6-20
pasting text A6-22
pin declarations A3-10, A3-16, A4-16, A7-6, A7-7, A9-20, A9-24, A/ApB-1
pin statement V14-7
printing file A6-3, A6-21
refreshing screen A6-5
reg keyword A3-16
replacing text A6-22
saving file and exiting A6-3
saving file changes A6-2, A6-20
saving file under new name A6-2, A6-20
searching for next-text-string instance A6-4
searching for text strings A6-4, A6-22
state keyword A3-11, A4-1, A9-21, A9-27
State statement V14-7
state table A3-3
state_diagram keyword A3-12, A3-18, A9-21
state_diagram statement V14-9
state_register keyword A3-11, A4-1, A9-20, A9-21, A9-27
state_register statement V14-7
state-machine encoding definitions A3-16
sync_reset keyword A3-12, A4-2
test vectors A3-13, A3-19, A9-25
test_vectors statement V14-9
title statement A3-10, A3-16, A9-20, A9-24, V14-6
undoing actions A6-22
Xilinx Property Dlc2p keyword A4-4
Xilinx Property Dlc2s keyword A4-4
Xilinx Property Dlp2p keyword A4-4
Xilinx Property Dlp2s keyword A4-4
Xilinx Property Initialstate statement V14-8

ABEL-HDL file *(Continued)*
Xilinx Property-Initialstate keyword A3-11, A3-12, A3-13, A3-18, A4-2
Xilinx Property-Map keyword A1-10, A4-3, A4-16, A9-3
Xilinx Property-Save keyword A4-3, A4-16, A9-1
Xilinx-Property-Initialstate keyword A9-20, A9-21, A9-28
ABL file A3-3
ABL2PLD
accessing through XDM R1-20
invoking A5-2
from operating system command line A5-8, A6-41
from XDM A5-8
options A6-41
-p A6-42
-r A6-42
purpose A1-6, A7-20
targeting PLD file to specific device A6-42
translating and assembling ABL file to PLD file A6-41
translating and integrating ABL file to PLD file A6-42
ABL2PLD command F2-20
ABL2XNF A1-6, M6-5, V6-10, V7-5, V14-10, V14-19, V14-23
accessing through XDM R1-20
controlling information output A6-39
disabling optimization A6-40
error messages A/ApA-1
families supported A6-39
help A6-39
invoking A5-1
from operating system command line A5-8, A6-38
from XDM A5-7
from XMake A5-7
optimizing for area A6-38
optimizing state machine speed A6-41
options A6-38
area A6-38
encode A6-38
family A6-39
help-all A6-39
listing A6-39
Maxclbs A6-39
memmiser A6-39
no-optimize A6-40
Old_library A6-40
output_directory A6-40
output_xnf A6-40
paramfile A6-40
part-type A6-40
sm_speed-opt A6-41
speed A6-41
unspecified_state A6-41
selecting encoding method A6-38
selecting library version A6-40
selecting part family A6-39
setting behavior of incomplete state machines A6-41
specifying maximum CLBs used A6-39
specifying output file directory A6-40
specifying output file name A6-40
specifying parameter file name A6-40
specifying part type A6-40
using less memory A6-39
ABL2XNF program
compiling Xilinx ABEL file O14-10
ACC L1-33, V5-11, V5-21
ACCUM module B4-2, B4-8
Adder/Subtracter B4-8, B4-9
ASYNC_VAL B4-11
RLOC_ORIGIN B4-12
RLOC_RANGE B4-12
STYLE
ALIGNED=Default B4-11
RPM B4-11
SYNC_VAL B4-11

ACCUM module *(Continued)*
TNM B4-12
USE_RLOC B4-12
Accumulator (ACCUM) B4-8
ACLK L1-19, L1-27, R2-114, R2-124
ACLK primitives U1-9
ACLK symbol V9-4, V11-89, V/ApE-20
active window R1-13
in XDM F2-6
ADD L1-33, V5-11, V5-21
add
add signals to waveform O16-52
default timing specifications O15-12
junctions O16-21
signals O16-28
stimulus editor O12-21
stimulus to schematic O12-6
trace to schematic O12-6
X-BLOX bus O13-5
X-BLOX module O13-3
ADD equation F4-44
add force M9-2
Add menu V/ApA-7
add property M3-7
ADD_SUB input
ADD_SUB module B4-14
ADD_SUB module B4-2, B4-14
RLOC_ORIGIN B4-16
RLOC_RANGE B4-16
STYLE
ALIGNED=Default B4-15
RPM B4-15
USE_RLOC B4-16
ADD_SUB symbol V13-10
add-attr command V3-6, V4-16, V11-97, V11-98, V11-100, V/ApA-11
add-box command V11-32, V/ApA-13
add-bus command V11-58, V16-19, V/ApA-12
add-comp command V4-15, V4-16, V11-45, V11-47, V11-68, V11-70, V11-141, V13-6, V15-11, V15-17, V16-16, V16-17, V16-26, V/ApA-8
adder/subtracter functions, see Xilinx Libraries Guide for description and selection details
adder/subtracter (ADD_SUB) B4-14
ADD-F-CI L1-102
ADD-FG-CI L1-103
ADD-G-CI L1-104
ADD-G-F1 L1-103
ADD-G-F3- L1-104
Adding
Module B2-1
add-label command V3-3, V11-34, V11-61, V11-74, V12-30, V16-23, V16-24, V16-25, V16-50, V/ApA-10
ADDMODE equation F4-46
add-net command V11-53, V16-20, V/ApA-7
add-pin command V11-33, V/ApA-13
ADDR
PROM B4-84
SRAM B4-107
ADDR_ERROR
PROM B4-85
SRAM B4-107
ADDR-ERR output R1-66
ADDSUB-F-C1 L1-108
ADDSUB-FG-CI L1-108
ADDSUB-G-CI L1-110
ADDSUB-G-F1 L1-109
ADDSUB-G-F3 L1-110
add-text command V11-40, V/ApA-14
ADI H1-9, R3-29
ADISTANCE option V/ApD-6, V/ApD-10, V/ApD-12
ADSU L1-33, V5-11, V5-21
after command V/ApB-21
AHDL2X A5-5, A9-34
case sensitivity A4-18
checking syntax errors A6-46

AHDL2X *(Continued)*
error messages A6-19, A6-36, A/ApA-2
functional simulation A9-26
options
-args A6-44
-blif A6-45
errlog A6-45
-list A6-45
-o A6-45
-ovector A6-45
-pla A6-45
-retain A6-46
-silent A6-46
-syntax A6-46
-vector A6-46
outputs A1-6, A6-11, A6-33
preserving redundant product terms A6-46
purpose A1-6
running on command line A5-9, A6-44
specifying compiler options file name A6-45
specifying error log file name A6-45
specifying list file format A6-45
specifying MODULE argument text A6-44
specifying output file format A6-45
specifying TMV file name A6-45
suppressing output messages A6-46
writing TMV file A6-46
AKA file M10-17, M10-28, V/ApD-1, V/ApD-2, V/ApE-4
Map2LCA R2-108, R2-112, R2-129
XNFCvt R1-106, R1-108
XNFMAP R2-55
aliases
*see also* NRF file
recycled aliases O10-24
signal name aliases O12-14
aliasing B2-22
all setting R2-38
guide_blks option R2-203
guide_routing option R2-203
guide_thru_routes option R2-178, R2-182, R2-183, R2-195, R2-204
ignore_locs option R2-191, R2-206
ignore_timespec option R2-197, R2-206
lock_routing option R2-178, R2-182, R2-183, R2-195, R2-207
allow block constraint R2-148
alternate directive A8-3
alternate-editor option A6-32
Altran V11-13
checking connectivity of WIR files V/ApF-7
displaying messages V/ApF-7
library privileges V/ApF-3
options V/ApF-4
-all V/ApF-5
-l V/ApF-6
-n V/ApF-6
-nocheck V/ApF-7
-p V/ApF-5
-s V/ApF-6
-v V/ApF-7
purpose V3-5, V/ApF-1
removing aliases V/ApF-4
syntax V/ApF-3
updating/changing aliases V/ApF-3
for read/write libraries V/ApF-5
for specific library V/ApF-6
for specific project components V/ApF-5
for specific schematic V/ApF-6
wildcards V/ApF-4
ALU function generator E5-28
ALU function generator (XC7272) E5-35
analyze
mode for XDelay O15-37
analyze mode V15-31
analyze option V/ApD-15

AND gates R2-5
AND gates,optimization F5-9
ANDBUS module B4-2
  attributes B4-3
  bused gate functions B4-4
ANDBUS1 module B4-2
  bused gate functions B4-4
ANDBUS2 module B4-4
ANDBUS2 symbol V13-10
annealing progress messages R2-161
Annotate
  accessing through XDM R1-20
annotate block type V10-26, V/ApA-18
annotate command F2-20
annotate program O3-8, O10-4
ANSI video interface
  XPP H4-7
Apollo F2-4
append command
  XPP H4-21
APR L1-34, R1-39, R2-131, R3-29, U3-2, U5-2, U5-3, V4-10, V7-1, V7-6, V7-11, V7-12, V10-5, V11-95, V11-116, V11-119, V11-139, V11-143, V11-144, V14-23, V15-1
  -a option R2-133
  accessing through XDM R1-24
  allow block constraint R2-148
  annealing phase R2-140
  annealing progress messages R2-161
  APRLoop R2-135
  area R2-146
  batch file for multiple runs R2-139
  block R2-146, R2-151
  block matching R2-134
  -c option R2-133, R2-145
  case sensitivity R2-132
  command options summary R2-138
  command–line syntax R2-131
  constraint files R2-144, R2-147
    case sensitivity R2-146
    syntax R2-148
  constraints R2-144, R2-147
    allow block R2-148
    definitions R2-146
    flag IOB R2-149, R2-155
    flag net R2-149
    include R2-149
    lock block R2-150
    lock IOBs R2-150
    lock net R2-151
    lock pin R2-151
    place block R2-151, R2-155
    place net R2-152
    prohibit block R2-152
    prohibit location R2-152
    summary table R2-154
    weight net R2-153
  CST file R2-133, R2-144, R2-145
  decrease net delays R2-136
  decrease program run time R2-137
  design files R2-141
    Apollo R2-142
    HP700 R2-142
    PC R2-142
    RS6000 R2-142
    Sun workstation R2-142
  DEV file R2-144
  device files R2-144
  evaluate routing effectiveness R2-138
  external IOB R2-146, R2-155
  flag IOB constraint R2-149, R2-155
  flag net constraint R2-149, R2-153
  -g option R2-133
  guided design R2-184
  improving results R2-154
  include constraint R2-149
  incremental design R2-134
  informational messages R2-155, R2-156
  input files R2-143
    CST file R2-144
    LCA file R2-143, R2-144

APR *(Continued)*
SCP file R2-143
summary R2-143
internal IOB R2-147, R2-155
interrupting R2-140
continue R2-141
quit R2-141
suspend R2-141
switch to next phase R2-141
-j option R2-135
-jpl option R2-139
-l option R2-135
LCA file R2-133, R2-139, R2-143
LCA guide file R2-144
leading path specifiers R2-142
-ljg option R2-139
location R2-146
lock block constraint R2-150
lock IOBs constraint R2-150
lock net constraint R2-136, R2-151, R2-154
lock pin constraint R2-151
locked block R2-147
message file R2-135
multiple runs R2-136, R2-139, R2-162
net R2-146
net matching R2-134
net weight R2-146
net–locked block R2-147
-o option R2-135, R2-161, R2-164
option combinations R2-138
options R2-132
add logic to LCA file R2-139
complete routing R2-138
constraints file R2-133
create report file R2-139
display all functions R2-137
-g R2-184
improve routing time R2-136
LCA file as guide file R2-133
lock blocks in place R2-135
-p R2-185
place design without routing R2-135
positioning on command line R2-132
preserve initial routing information R2-136
redirect message output R2-135
routing attempts R2-133
set router type R2-136
set seed for multiple runs R2-136
skip annealing algorithm R2-136
summary R2-138
suppress overwrite warning R2-137
use faster placement R2-137
useful combinations R2-138
options summary R2-137
OUT file R2-135
output file R2-156
output files R2-155
LCA file R2-156
OUT file R2-156
RPT file R2-156
summary table R2-156
-p option R2-136, R2-147, R2-151
package information files R2-144
pin R2-146, R2-151
pin matching R2-134
PKG file R2-144
-pl option R2-138
place block constraint R2-151, R2-154, R2-155
place net constraint R2-152
placing larger designs R2-162
prohibit block constraint R2-152
prohibit location constraint R2-151, R2-152
purpose R1-4
-q option R2-136
quenching phase R2-140

APR *(Continued)*
quitting current run R2-141
-r option R2-136
report file R2-156
block placement and pin swapping table R2-158
delay table R2-160
final results summary R2-158
header information R2-157
load pins R2-161
net delay table R2-159
net routing order R2-158
net status R2-160
net, block, and location flags tables R2-159
source pins R2-160
unrouted nets listing R2-158
routing larger designs R2-162
routing phase R2-141
continue R2-141
quit APR run R2-141
suspend R2-141
write report file R2-141
RPT file R2-139
running APR in background R2-140
running on RS6000 R2-142
running on Apollo R2-142
running on HP700 R2-142
running on PC R2-142
running on Sun workstation R2-142
-s option R2-136
SCP file R2-143, R2-144, R2-145, R2-155
SPD file R2-144
speed information files R2-144
-t option R2-136
timing improvment R2-136
use with XDM R2-131
-w option R2-137
weight net constraint R2-153
-x option R2-137
-y option R2-137
APRLoop R2-135, R2-141, R2-162, U5-3
accessing through XDM R1-24
command–line syntax R2-162
design iterations R2-163
interrupting R2-163
-o option R2-164
options R2-163
OUT file R2-164
redirecting output R2-164
terminating R2-163
architectural resources U2-2
architecture
and design constraints F5-7
mapping design to F5-9
archopt option B/Ap-1, V10-9
area R2-146
area option A1-9, A6-9, A6-25, A6-38, A9-5
args option A6-44
ARITH style B4-34, B4-97
arithmetic
carry enable equation
ADD F4-44
ADDMODE F4-46
carry-in F4-44
design examples
4-bit adder E5-30
8-bit adder/subtracter E5-33
adder/subtracter (XC7272) E5-39
design rules E5-28
logic architecture E5-28
XC7272 E5-35
arithmetic carry logic A7-1
arithmetic functions, see Xilinx Libraries Guide for description and selection details
arrays V/ApA-25
arrow keys
activating F2-38
defining in XDelay R3-23
defining in XDM R1-33
ASCII A1-9, A6-13, A6-28, V16-10, V/

ApA-16, V/ApA-17, V/ApA-19, V/ApA-27
ASCII-wave option A6-28
ASCTOVST
accessing through XDM R1-26
ASCTOVST command F2-29
ASCTOVST program O10-25, O12-17
assemble PLD File command A5-8
assembler-log report V16-35
assembler-error report V16-35
assembling an equation file F2-22
Assign menu V/ApB-14
AST file O6-4, O8-4, O10-20
ASYNC_CTRL B2-9
ACCUM B4-10
CLK_DIV B4-29
COUNTER B4-38
DATA_REG B4-49
SHIFT B4-96
async_reset keyword A4-2
ASYNC_VAL attribute B2-8, B2-9
ACCUM B4-11
COUNTER B4-39
DATA_REG B4-50
SHIFT B4-97
usage B2-8
asynchronous control B2-8
asynchronous latches A1-12
asynchronous peripheral mode U6-19
asynchronous reset equation (RSTF) F4-59
asynchronous set equation (SETF) F4-60
ATR file O6-4, O8-4, O10-20
attribute
F schematic E4-12
attributes
$ARRAY V/ApA-9
@PULSEH V9-5
@PULSEHI V9-4
@PULSEL V9-5
@PULSELO V9-5, V/ApE-23
*see also* symbol, signal attributes
ABLE
EPLD A7-13
adding O4-3, O4-7, O16-25
assignment A4-5
ASYNC_VAL B2-9
BASE V4-8
BLKNM V4-3, V15-7, V15-18
BOUNDS B2-17, V6-8, V6-9, V13-8, V13-9
buffer A4-6, A7-14
CAP V4-8
changing text size in ViewDraw V11-38
CLB V4-8
CLOCK_OPT V5-8, V5-19
CMOS V4-8
com A4-6, A7-14
component V5-14
CONFIG V4-8
COUNT_TO B4-40
custom macro symbols V5-15
DECODE V4-4
DECODEMASK B2-9
DEF V13-9, V14-15
DEPTH B4-85, B4-107
DEVICE V15-12
devices supported V4-2
DIVIDE_BY B4-30
dot extensions A4-6, A7-14
DOUBLE V4-4
DUTY_CYCLE B4-30
ELEM B4-60
ENCODING B2-16, V13-8, V13-9
entering V3-6, V11-36
entering X-BLOX V4-16, V13-9
EPLD V5-14
EPLD attributes
CLOCK_OPT O5-22
component O5-16
FOE_OPT O5-22
global O5-16
LOGIC_OPT O5-21

attributes *(Continued)*
LOWPWR=ALL O5-21
MINIMIZE O5-21
MRINPUT O5-21
PARTTYPE O5-16
PRELOAD_OPT O5-22
REG_OPT O5-22
signal O5-16
UIM_OPT O5-21
EQUATE_F V4-8
EQUATE_G V4-8
EXT V11-96
FAST V4-7, V11-99, V/ApE-2
FAST3KA B5-3
FILE V1-4, V3-10, V4-3, V6-3, V6-7, V6-8, V14-15, V14-21, V/ApE-3
FLOAT_VAL B2-12
FOE_OPT V5-18
FPGA attributes
external I/O O4-4
PARTTYPE O4-9
pin O4-3
signal O4-5
symbol O4-4
table of O4-13
TIMEGRP O4-8
TIMESPEC O4-7
TNM O4-9, O15-11
user O4-6
global V5-14, V5-17
HBLKNM V4-4, V15-7
HU_SET V4-6
implementation style B2-4
INC_BY B4-65
INIT V4-4, V9-2, V12-18, V/ApB-24
input/output V4-7
INV V/ApE-10
invert A4-6, A7-14
INVMASK B2-9, V13-11
bus–level functions B2-9
IOB V4-8
KEEPNAME (KN) B2-23
LEVEL V5-13, V11-82, V15-12, V/ApD-12
LIBVER V11-82, V11-96, V13-9, V15-12
LOC B2-27, V4-5, V5-16, V11-96, V11-115, V15-10, V16-27, V/ApE-3
LOGIC_OPT V5-17, V5-18
LOWPWR V5-16, V5-17
MAP V4-4, V/ApE-1
MEDFAST V4-7, V11-100
MEDSLOW V4-7, V11-100
MEMFILE B4-85
minimize V5-18
MRINPUT V5-18
narrow_menus V11-17
neg A4-6, A6-11, A6-27, A7-14, A7-15, A7-16
net attributes
adding O11-55
net *see* net attributes
no_look V11-17
NODELAY V4-7
operating modes B2-6
OPT V5-17, V9-7
overlap V11-17
PART V4-11, V5-20, V11-94, V16-26, V/ApD-17
PARTTYPE O11-53
PINTYPE V4-12, V10-3, V11-36, V11-39, V11-96, V/ApE-11, V/ApE-18, V/ApE-22, V/ApE-23
PLD V5-10, V5-13, V5-15
pos A4-6, A6-11, A6-27, A7-14, A7-15, A7-16
PRELOAD_OPT V5-19, V9-6, V16-26
PULLUP B4-111
purpose V4-1, V5-14
reg A4-6, A7-14
reg_d A4-6, A7-14
reg_g A4-6, A7-14
reg_jk A4-6, A7-14

attributes *(Continued)*
reg_opt V5-8, V5-19
reg_sr A4-6, A7-14
reg_t A4-6, A7-14
RES V4-8
RIPPLE B5-3
RLOC V4-6, V11-85
RLOC_ORIGIN B5-3, B6-10, V4-6
RLOC_RANGE B5-4, B6-10, V4-6
schematic E4-12
see properties
sheet symbol V10-26
SLICE B4-103
SLOW V4-7
specifying attributes B3-7
STYLE B4-3, B5-1
SUB B4-103
SUB_STARTS_AT B4-103
SYNC_VAL B2-9
TNM B2-31, V4-9
TS V4-9
TSidentifier B2-31, V4-9
TTL V4-8
turning off visibility V11-39
U_SET V4-6
UIM_OPT V5-18
USE_RLOC B5-3, V4-6
VALUE B4-63
ViewGen V/ApD-14, V/ApD-17
Viewlogic-specific V4-11
XACT-Performance V4-9
XOR A7-14
AUTHOR keyword V16-29
author statement E2-2
auto parameter R1-82, R1-85
auto setting
dc2p option R2-196, R2-199
dc2s option R2-199
dp2p option R2-201
dp2s option R2-201
autoexec.bat, path statement for XDM F2-2, F2-4
autoexec.bat file O2-4, V11-4, V11-5, V12-4, V12-6, V16-6
auto-make-options dialog box A6-31
Automatic Place and Route program R1-4, R2-131
Automatic Place and Route Program *see* APR
automatic translation
EPLD implementation O7-7
FPGA implementation O7-4
functional simulation O6-1
timing simulation O8-1
XEMake
command summary O7-10
flow chart O7-8
subprograms O7-10
XMake
Command summary O7-6
flow chart O7-3
Subprograms O7-6
subprograms O8-5
XSimMake
subprograms O8-5
automatically update viewer windows A6-31
auto-polarity option A6-11, A6-27, A7-16

## B

back-annotation B3-8, B3-12, M8-1, M10-15, R3-30, U1-15, V6-3, V6-10, V8-2, V9-5, V9-7, V9-8, V10-11, V10-14, V10-18, V10-20, V10-21, V12-1, V12-6, V12-22, V12-23, V12-25, V12-34, V12-49, V12-51, V12-56, V13-21, V13-22, V13-23, V14-21, V14-24, V14-25, V14-26, V16-39, V16-44, V16-45, V/ApA-14, V/ApC-13, V/ApD-3, V/ApD-4, V/ApE-3, V/ApE-10, V/ApE-11, V/ApE-12

backslash V11-3, V16-10
BASE attribute V4-8
  architectures L1-2
  purpose L1-2
  syntax L1-4
  XC2000 modes L1-2
  XC3000 modes L1-2
BASE field O4-11
base memory
  XC4000 Demonstration Board H2-2
BASE property M4-9
bat file
  XPP H4-17
BAX
  error messages R3-50
  warning messages R3-49
  XC2000 and XC3000 designs
    inputs R3-48
    outputs R3-48
    syntax R3-48
behavioral design E1-1, F/ApC-11
  Boolean equation entry E1-2
  bus and vector operations E1-3
  getting started E1-1
  hierarchical format E1-1
  integrating F2-24
  overview F1-9, F1-10
BIDIR_IO module B4-2, B4-18
  BOUNDS B4-19
  ENCODING B4-19
  FLOAT_VAL B4-20
  LOC B4-20
  PADNAME B4-20
  TNM B4-21
bidirectional I/O (BIDIR_IO) B4-18
  assigning signals E4-14
bidirectional I/O pin O5-5
bidirectional pins A1-12, V5-5
big–endian B2-18
binary B2-8
binary counter B4-40
binary encoding A3-6, A6-9, A6-25, A6-38, A6-42, U3-4
  EPLDs A3-6, A3-7
  FPGAs A3-6
binary point B2-18
BIT encoding B2-17
BIT file M7-1, M7-4, M7-7, O7-1, V7-1, V7-2, V7-6, V11-119, V13-21, V14-23, V14-24
  MakeBits R2-228
  MakePROM R1-5, R2-270, R2-275
  XDE R3-65
  XMake R1-3, R1-39
  XPP H4-2, H4-10
bitfiles
  creating U6-3
  loading U6-4
  saving U6-4
bit-maps
  files E1-11
  in library F5-13
bits per frame U6-40
bitstream M11-101, U1-13, V7-12, V7-14, V11-1, V11-2, V11-10, V11-12, V11-13, V11-14, V11-118, V11-119, V11-130, V11-134, V11-136, V11-145, V11-146, V11-148, V11-149, V11-150, V13-12, V13-18, V13-20, V14-16, V14-21, V14-23, V15-23
  creating U6-5
  daisy chain U6-5
  downloading to an FPGA O11-91
  generation U1-15, U3-7
  header U6-4
  single device U6-5
bitstreams
  ASCII R2-259
  configuration options in XMake R1-39
  creating R1-5
  creating in LCA file R2-243, R3-145
    XC3000 Demonstration Board H1-13

bitstreams *(Continued)*
XChecker H5-9
creating with XMake H5-10
download port selection R2-261
downloading to cable in XDE R3-119, R3-124
downloading to cable with XChecker H5-4
downloading to LCA device R2-253
generating multiple R2-227, R2-238, R2-243
generating with MakeBits H2-13, R2-227, R2-244, R2-256
FPGA Demonstration Board H3-25
loading in MakePROM R2-278
mask file R2-238, R2-260
pins required for downloading H2-6
place in design implementation R1-2
readback R2-249
reading file R2-265
reading file in XDE R3-168
renaming file R2-238
saving R2-269
saving configuration in XDE R3-193
tied R2-267
use with Rawbits R2-265
BL0 file A1-6, A1-8, A5-4, A6-11, A6-16, A6-31, A6-33, A6-45, A6-46
BL1 file A1-8
blif option A6-45
BLIFOPTX A5-5
help A6-46
minimizing product terms A6-8, A6-24, A6-47
options
-errlog A6-46
-help A6-46
-o A6-47
-pla A6-47
-reduce A6-47
purpose A1-6
running on command line A5-9, A6-46
specifying error log file name A6-46
specifying output file format A6-47
specifying output file name A6-47
BLKNM attribute L1-4, L1-47, O4-14, V4-3, V15-7, V15-18
architectures L1-4
Place Block constraint L1-49
purpose L1-4
symbols L1-5
syntax L1-6, L1-46
BLKNM parameter R2-61
BLKNM property M4-3, M4-4
block R2-146
export O11-41
import O11-42
block name (BLKNM) field O4-11
block placement U2-5
blocks
assigning names R3-150
coloring in XDE R3-104
configuring logic and connections in XDE R3-105
copying configuration in XDE R3-114
deconfiguring in XDE R3-103, R3-120
delays R3-29
deselecting in XDE R3-130
displaying configuration information in XDE R3-102
displaying information on saved blocks in XDE R3-168
displaying scrolling menus in XDE R3-102
editing comment text in XDE R3-126
ending points for path delay in XDelay R3-6
flagging for path delay calculator in XDE R3-138
flagging for use by path delay calculator in XDelay R3-18
guided placement R2-181

blocks *(Continued)*
highlighting connections in XDE R3-185
including block-only information in XNF file in LCA2XNF R3-30
invalid name in LCA file R3-36
moving configuration and net connections in XDE R3-148
moving window to in XDE R3-137
multiple base/config records R3-36
removing connections from world view in XDE R3-192
requesting information in XDE R3-159
restoring saved information in XDE R3-171
routing pins in XDE R3-172
saving information to text file in XDE R3-171
saving to temporary space in XDE R3-175
starting points for path delay in XDelay R3-6
swapping groups in XDE R3-188
swapping net connections in XDE R3-186
tagging with text in XDE R3-104
unconfigurable R3-36
unrouting pins in XDE R3-191
BLX file V13-13, V13-17
blxfile option B/Ap-1
Boolean equations E1-1, V16-29
Boolean expressions R1-2, R3-46
Boolean minimization L1-31
Boolean operators
XC2000 L1-12
XC3000 L1-12
border symbols V/ApD-9
boundary scan R2-248, U7-4, U7-9, U8-1
availability U8-11
bibliography U8-19
BSCAN primitive U8-14
BSDL U8-19
bypass U8-17
bypass register U8-9
CLBs U8-17
configure U8-17
data register U8-5
data-register cell U8-7
deviations from IEEE standard U8-2
DRCK U8-10
Extest U8-3, U8-15
features U8-2
global clock inputs U8-7
hardware U8-3
IDLE U8-10
IEEE Standard 1149.1 U8-2
instructions U8-5, U8-15
Intest U8-16
IOBs U8-2, U8-5
logic in IOBs U8-6
loop U8-1
order U8-9
path U8-1
pins U8-7
post configuration U8-14
readback U8-18
resistors U8-7
sample/preload U8-16
SEL1 U8-10
SEL2 U8-10
start-up sequence U8-12
TAP pins U8-3
TDO1 U8-10
TDO2 U8-10
use U8-1
user registers U8-10
User1 U8-17
User2 U8-17
using U8-11
using with XDE U8-15
Boundary Scan Description Language *see* BSDL

BOUNDS attribute V6-8, V6-9, V13-8, V13-9
  BIDIR_IO B4-19
  BUS_DEF B4-22
  CAST B4-27
  COUNTER B4-41
  data type propagation B2-19
  DATA_REG B4-50
  FORCE B4-62
  INPUTS B4-69
  OUTPUTS B4-81
  PROM B4-86
  SHIFT B4-98
  SLICE B4-103
  SRAM B4-108
  usage B2-17
BPAD L1-5
break command V12-44
break option A6-48
BreakLoop option
  using in XDelay R3-25
breakpoint V/ApB-8, V/ApB-9
brief option A6-29
brief trace option A6-14
bring-transcript-to-front option A6-31
browse
  accessing through XDM R1-29
browse command F2-34, F3-1
Browse menu
  command E3-9
BSCAN primitive U8-14
BSDL U8-19
bubble diagrams A3-1
BUF V5-6, V11-142
BUFCE V5-11
BUFE L1-15, V5-3, V5-6, V5-11, V5-18, V5-21
buffer attribute A4-6, A7-14, A/ApB-1
buffer functions, see Xilinx Libraries Guide for description and selection details
Buffer menu V/ApC-9
buffer-append command V/ApC-11
buffer-copy command V/ApC-9
buffer-cut command V/ApC-10
buffer-paste command V/ApC-10
BUFFOE V5-2, V5-3
BUFFOE component E4-12, E4-13
BUFG M5-7, V5-2, V5-7, V16-18
BUFGP L1-19, L1-27, L1-54, L1-70, L1-71, V11-91, V/ApE-20
BUFGP primitives U1-9, U3-8
BUFGS L1-19, L1-27, L1-54, L1-70, V11-91
BUFGS primitives U1-9, U3-8
BUFT L1-20, L1-67, V3-2, V4-3, V4-5, V4-6, V5-6, V5-11, V7-6, V10-11
  constraints L1-67
  LOC placement examples L1-26
  placement constraint syntax L1-52, L1-54
  use with BLKNM attribute L1-5
  use with DECODE attribute L1-11
  use with DOUBLE attribute L1-12
  use with HBLKNM attribute L1-16
  use with LOC constraint L1-19, L1-21, L1-72
  use with net attributes L1-33
  use with RLOC constraint L1-40, L1-72
  use with RLOC_ORIGIN constraint L1-41, L1-86
  use with RLOC_RANGE constraint L1-89
BUFT symbols R1-111
builtin library V2-5, V2-7, V2-12, V3-8, V11-9, V11-14, V11-80, V/ApF-2
buried nodes A4-16
buried-node numbers A4-16, A7-20, A8-2
bus
  Bidirectional data B4-110
  big–endian, little–endian B2-18
  Constant B4-2
  data type B2-16
  ELEMENT of a bus B4-2

bus *(Continued)*
HIGH SLICE, example B4-104
interface B2-28
labels B2-15
LOW SLICE, example B4-104
manipulation B2-25
CAST symbol B2-25
ELEMENT symbol B2-26
FORCE symbol B2-26
MUXBUS symbol B2-27
SLICE symbol B2-26
MID SLICE, example B4-104
naming buses O11-34
placing buses O11-28, O11-40
width B2-17
X-BLOX buses O13-6
bus definition symbols V13-7
bus notation R1-64
bus pad symbols L1-21
bus pins R2-14
bus rippers M3-5
RULE property M3-6
BUS_DEF module B2-21, B2-29, B4-2, B4-22
BOUNDS B4-22
ENCODING B4-22
BUS_DEF symbol V13-7, V13-9
BUS_IF symbols B2-28, V4-16, V13-7
bused-gate functions B4-2, B4-4
ANDBUS2 B4-4
INVBUS B4-5
ORBUS B4-5
ORBUS1 B4-6
ORBUS2 B4-6
XORBUS B4-6
XORBUS1 B4-7
XORBUS2 B4-6, B4-7
buses
adding attribute text V/ApA-11
adding labels V11-62, V16-24, V/ApA-10, V/ApA-12
adding to schematic V11-58, V16-19, V/ApA-12
bidirectional V4-4
bounding boxes V/ApA-23
combining signals in ViewWave V/ApC-16
connecting to nets V/ApA-8
dangling V/ApA-12
defining as vectors V12-16
deleting V/ApA-32
displaying in ViewWave V12-39, V/ApC-14
dividing in ViewWave V/ApC-16
ending in schematic V/ApA-12
expanded notation in WIR2XNF V3-3
monitoring during simulation V12-12
naming conventions V3-1, V3-3
naming in ViewGen V/ApD-9
output data V16-44, V16-45
selecting label name V/ApA-30
simulation V6-3, V6-10, V8-2
specifying in ViewWave stream V12-13
stretching V/ApA-29, V/ApA-33
vectors V14-7
X-BLOX V4-16, V6-8, V12-34, V13-6, V13-13, V13-16
busname option V/ApD-9
button settings on mouse F/ApC-8
Bye menu V/ApA-38
bye-quit command V11-16, V11-25, V11-114, V11-142, V12-28, V12-47, V12-56, V16-1, V16-11, V16-28, V16-54, V/ApA-38
bypass U8-11, U8-13, U8-16, U8-17
bypass register U8-9

## C

C net attribute L1-33, V4-10
C_IN
ACCUM B4-9
ADD_SUB B4-14
C_OUT

ACCUM B4-11
ADD_SUB B4-15, B4-65
c2p R1-86, R1-89
overlapping specifications R1-90
c2s R1-86
clock period R1-87
high time R1-87
overlapping specifications R1-87
c2s specifications R2-196, R2-215, R2-219
calc_da M11-9
cancel button A2-4
CAP attribute O4-14, V4-8
architectures L1-6
purpose L1-6
symbols L1-6
syntax L1-7
CAP property M4-9
capacitive mode L1-6, L1-40, V4-8
carry logic L1-96, L1-97, M3-4, R2-38, R2-42, R2-184, R2-191, R2-205, R2-207, V1-2, V11-85
carry mode configuration mnemonics L1-101
carry mode names and symbols L1-99
carry mode primitive symbols L1-98
dedicated L1-98
handling in XNFPrep L1-100
LOC constraints L1-99
primitives L1-98
RLOC constraints L1-99
carry-logic symbols R1-111, R1-117
carry-mode configuration mnemonics L1-101
carry-mode names and symbols L1-99
carry-mode primitive symbols L1-98
cascading counters B4-45
case sensitivity A4-18
CAST module B4-2, B4-24
BOUNDS B4-27
ENCODING B4-27
CCLK V3-2
CCLK speed (XC4000 only) R2-248
CD-ROM V13-2, V14-2, V15-2
CE
design rules F5-8
CEPIN statement E2-3, F4-5, F4-6
cerify-vmh2xnf command A7-23
Change menu V/ApA-20
change-array command V/ApA-25
change-attr-dialog-all command V3-6, V3-10, V4-16, V11-37, V11-86, V11-94, V11-96, V11-97, V13-9, V14-15, V15-11, V15-12, V15-14, V15-15, V15-16, V15-17, V15-19, V16-25, V16-26, V16-27, V16-47, V/ApA-21, V/ApE-20, V/ApE-23
change-attr-invisible command V11-39, V11-82, V/ApA-22
change-attr-visible command V11-39, V11-82, V/ApA-22
change-block-sheet command V11-32, V/ApA-20
change-block-type command V3-9, V14-14
change-comp command V11-66, V11-91, V11-93, V11-105, V11-110, V13-4, V14-13, V16-50, V/ApA-26
change-display-context-off command V11-28, V/ApA-23
change-display-context-on command V/ApA-23
change-display-values command V12-23
change-grid-off command V/ApA-23
change-grid-on command V/ApA-23
change-grid-space command V/ApA-24
change-label-invisible command V/ApA-20
change-label-sense command V3-2, V/ApA-21, V/ApD-2
change-label-visible command V/ApA-20
change-pin-sense command V/ApA-23
change-text-size command V11-38, V11-40, V11-94, V11-96, V/ApA-24
change-text-string command V11-40,

V11-43, V11-61, V16-48, V/ApA-25
check boxes A2-4
check command V/ApB-22
XPP H4-20
Check program V3-7, V3-9, V11-1, V11-51, V11-52, V11-112, V11-121, V12-8, V13-14, V13-15, V14-19, V14-20, V/ApF-7
checker, for design rule violations F5-7
checking schematics O16-35
checksum command
XPP H4-20
chip builder integrator module F5-7
CHIP keyword V5-13, V5-15, V16-29
chip statement E2-2, E4-3, E4-4
chref M2-8
CIN pin L1-100, L1-101
CIN pin *see also* individual carry mode configuration mnemonics
circuit event V/ApB-9, V/ApB-10
CIRCULAR style B4-97
class P symbols M1-8
CLB M6-5, M8-3, M10-3, M10-5, M10-14
Asynchronous Set/Reset R3-19
computing number B6-7
SRAM CLB utilization B4-109
CLB limit option A1-10, A6-9, A6-25
CLB primitives
functional simulation O10-13
CLB RAM R3-19, R3-139
DATA inputs R3-19
CLB/IOB properties
modifying M4-9
see also properties
CLBMAP L1-20, L1-59
closed L1-62
locked pins L1-62
mapping constraints L1-61
open L1-62
unlocked pins L1-62
use with BLKNM attribute L1-5
use with HBLKNM attribute L1-16
use with LOC constraint L1-19
use with MAP attribute L1-29
use with net attributes L1-34
use with Place Block constraint L1-49
CLBMAP constraints L1-61
CLBMAP symbol U2-4
CLBMAP symbols R2-22, R2-43, R2-47, R2-50, R2-57, R2-87, R2-120, R2-184
guided design R2-55
CLBMAPs V/ApF-7
LOC constraints V4-5
MAP attribute V/ApE-1
pins V4-10
primitives V4-10
symbols V4-3, V4-4, V15-10, V/ApE-1, V/ApE-2, V/ApF-7
CLBs A1-10, A1-11, A6-9, A6-25, A6-38, A6-39, A6-41, A6-44, A9-3, L1-55
adding interconnects R2-240
aligning inputs with longline L1-34
assigning block names to primitives R2-61
attributes V4-8
BASE attribute V4-8
base configuration L1-2
BLKNM attribute V4-3
block definition L1-47
CLBMAP constraints L1-61
CLBMAP symbols R2-57
clocks L1-33, V4-10, V9-3
combinational logic L1-35
CONFIG attribute V4-8
configuration tags
XC2000 R3-109
XC3000 R3-109
XC4000 R3-110
configured pins unconnected to nets R3-33
configuring carry logic in XDE R3-113
configuring logic functions R3-132
constraints L1-63

CLBs *(Continued)*
dedicated carry logic L1-98, L1-101
direct flip–flop input pins R2-46
EQUATE_F attribute V4-8
EQUATE_G attribute V4-8
feed-through R3-44
FILE= attribute R2-48
flattening before mapping in XMake R1-42
flip-flop clock inputs R3-34
flip-flop constraints L1-55
flip-flop data pins R3-34
flip-flop hold violations V9-2
flip-flop setup times V9-3
flip-flops R3-44, R3-45, V4-9
function generators R2-46, R2-61
illegal configuration R3-39
illegal value on base record R3-36
incorrectly specified symbol R3-37
input signals V9-3
invalid location in MAP file R2-114
loadless R3-34, R3-35
LOC constraint R1-113, V4-5
LOC constraint examples L1-24
location constraints R2-10
logic configuration U7-4
mapping R2-50
mapping by FMAPs V11-85
mapping by XMake V11-1
mapping by XNFMAP V7-6, V10-11, V11-144, V11-148
mapping gates into function generators L1-46
mapping with BLKNM attribute L1-5
multiple–block placement R2-63
on-chip memory V11-104, V11-105
ordering logic function inputs in XDE R3-152
pairing flip–flops R2-50, R2-61
partitioning in XNFMap R2-168, R2-177
pin swapping L1-29
Place Block constraint L1-49
placement R2-146, R2-148
preventing net absorption V11-97
primitive symbols R2-5
primitives R2-102, R3-36, V4-5, V6-7, V6-11, V10-5, V10-6, V10-9, V10-10
prohibit location R2-152
prohibiting logic placement L1-21
reducing number in XNFMAP R2-48
register ordering R2-50
relax signal–combining requirements R2-49
removing unused in LCA2XNF R3-32
representing internal nodes R2-176
reserved names V3-2
restrictions V15-31
ROM and RAM constraints L1-57
S net attribute V4-10
setting constraint file flag in XDE R3-146
setting logic equations for function generators L1-12
single–block placement R2-63
specifying functions with CONFIG attribute L1-8
symbols L1-16, L1-20, V4-3, V/ApF-7
through-routes R2-183, R2-193
unconfigured R3-34
use with BLKNM attribute L1-5
use with LOC constraint L1-19, L1-21, L1-72
use with RLOC constraint L1-73
viewing in XDE V11-127
X net attribute V4-10
XC2000 U1-4
XC2000 configuration options L1-9
XC2000L U1-4
XC3000 U1-3
XC3000 configuration options L1-10
XC3000A U1-3

CLBs *(Continued)*
XC3000L U1-3
XC3100 U1-3
XC3100A U1-3
XC4000 carry logic R3-40
XC4000 function generators R3-40, R3-43, R3-44, R3-46
cleanup
accessing through XDM R1-21
cleanup command F2-20, V/ApA-39
cleanup utility O11-70, O15-27
cleanupX A1-7, A5-10
clear (asynchronous) E2-11
ClearOptions V15-33, V15-40
clear-template option V15-28, V15-31
CLIB directory F5-13
subdirectory V5-15, V7-10, V16-34
CLK U7-7
CLK_DIV attribute
DIVIDE_BY B4-30
CLK_DIV module B4-2, B4-28
DUTY_CYCLE B4-30
TNM B4-30
CLK_EN
COUNTER B4-38
DATA_REG B4-49
SHIFT B4-95
CLK_OUT
CLK_DIV B4-29
CLKF equation F4-48
CLOCK
ACCUM B4-10
CLK_DIV B4-29
COUNTER B4-38
DATA_REG B4-49
SHIFT B4-96
clock V4-10, V5-2, V5-7, V5-19, V9-3, V9-4, V9-6, V11-29, V11-52, V11-88, V11-91, V11-106, V11-121, V11-127, V12-16, V12-19, V12-42, V14-8, V14-9, V15-6, V15-7, V15-9, V15-11, V15-12, V15-28, V15-40, V15-42, V16-40, V/ApB-6, V/ApB-7, V/ApB-8, V/ApB-19, V/ApD-5, V/ApE-4
clock buffers L1-19, V1-2, V3-2, V7-6, V10-11, V11-88, V11-89, V11-90, V11-91, V11-128, V11-129
clock divider (CLK_DIV) B4-2, B4-28
clock enable U3-9
Clock Enable see CE
clock nets R3-14, R3-17, R3-27
ending point for path search in XDelay R3-7
starting point for delay path in XDelay R3-7
used in timing analysis R3-15
clock option A6-29
clock paths R3-177
CLOCK_OPT attribute O5-22, V5-8, V5-19
architectures L1-7
purpose L1-7
syntax L1-7
CLOCK_OPT property M5-17, M5-21
clock_period parameter R1-87
clocks
default E4-13
FastCLK E3-18, E4-9
maximum frequency calculation E5-10
product term E3-17
clock-to-output time calculation E5-9, E5-13, E5-19
ClockToPad option V15-29, V15-39
clock-to-pad path delay V15-11, V15-12, V15-20, V15-33
clock-to-pad paths R2-196, R2-198, R2-218
ClockToSetup option V15-29, V15-39, V15-40
clock-to-setup path delay V15-6, V15-12, V15-20, V15-33
clock-to-setup paths R2-196, R2-199, R2-218
clock-trace option A6-14
CMD file V12-45

CMOS attribute O4-14, V4-8
architectures L1-8
output drive levels L1-8
purpose L1-8
symbols L1-8
syntax L1-8
CMOS input signal threshold R2-229
CMOS property M4-9
color command V/ApC-26
Color menu V/ApC-26
colors of menu
changing arrangement F2-39
changing palette F2-40
com attribute A4-6, A7-14
comand
compile
options A6-5
combinational equations E2-12, E2-15
combinational logic A1-10, A3-4, A3-12, A9-21, A/ApB-1
combinational loops R1-82
combinatorial paths R3-9
command (see also, commands)
compile
options A5-4, A5-7, A6-11
parse ABEL source A6-11
simulate equations A5-5
trace options A5-4
Xilinx EPLD netlist A6-10
Xilinx EPLD options A6-10
Xilinx FPGA netlist A6-7
Xilinx FPGA options A6-7
edit
delete line A6-4
edit A5-3
next A6-4
replicat line A6-4
search A6-4
file
DOS shell A6-3
exit A5-3, A5-9, A6-3
insert A5-3, A6-2
new A6-1
open A5-3, A6-2
print A5-3, A6-3
save A5-3, A6-2
save as A5-3, A6-2
save options A6-2
save-and-exit A6-3
fitter fiteqn A5-9
my text editor is A5-3, A6-5
options
auto make A5-4
auto update A5-4
compile A5-4
compile listing file A5-7
editor A5-3
simulate A5-4
show any file A5-7
show compiled equations A5-7
show compiler listing A5-7
show error log A5-3, A5-6
show simulation results A5-5, A5-6
view compiled equations A5-7, A6-6
view compiler listing A5-7, A6-5
view errors A5-3, A5-6, A6-6
view file A5-7, A6-6
view simulation results A5-5, A5-6, A6-6
view Xilinx EPLD equations A6-6
view Xilinx SYNTHX report A6-6
command buttons A2-4
command file V9-7, V9-8, V9-9, V11-10, V12-28, V12-35, V12-39, V12-44, V12-45, V12-52, V13-18, V16-40, V/ApB-20, V/ApC-7, V/ApC-11, V/ApC-17, V/ApD-5
executing from XDM R1-31
command line interface R1-18
command line interface of XDM F2-9
command syntax B/Ap-1

commands O11-13
ABL2PLD F2-20
annotate F2-20
ASCTOVST F2-29
browse F2-34, F3-1
cleanup F2-20
cursor F2-38
DirClean F2-34
directory F2-34, F/ApC-9, F/ApC-10
DOS F2-35
edit F2-35, F3-1
entering commands O11-13
entering using keyboard F2-9
entering using mouse F2-9
executing with a function key F2-38
family F2-38
FITEQN F2-24
example F/ApC-20
FITNET F2-25, F5-3
JED2PLD F2-22
KeyCursor F2-38
keydef F2-38
example F/ApC-9
MAKEJED F2-31
MAKEPRG F2-32
example F/ApC-22
menucolors F2-39
mouse F2-39
options F2-39
PALCONVT F2-26
palette F2-40
part F2-40
pinsave F2-18, F2-23, F/ApC-20, F/ApC-22
PLUSASM F2-22
printer F2-40
PROLINK F2-33, F/ApC-22
readprofile F2-40
repeating F2-9
saveprofile F2-40
SDT2NET F2-21, F5-15
selecting F/ApC-7
settings F2-40
speed F2-40
summaries O11-102
using shortcuts F2-9
version F2-37
VMH2VST
example F/ApC-23
VMH2WIR F2-32
example F/ApC-23
VSM F2-30
example F/ApC-23
WIR2NET F2-21, F5-15
XDM, entering F2-8
XNF2VST F2-29
XNF2WIR F2-31
XNFMERGE F2-23
XSIMMAKE F2-28
COMP property M4-1, M4-2
COMPANY keyword V16-29
company statement E2-3
comparator functions, see Xilinx Libraries Guide for description and selection details
compare command
XPP H4-20
COMPARE module B4-2, B4-32
equality B4-32
magnitude B4-32
RLOC_RANGE B4-34
STYLE B4-34
ARITH B4-34
RIPPLE B4-34
TREE B4-34
WIRED B4-34
comparison logic U7-4
compcomp option V/ApD-10
Compile menu
PCs A6-6
workstations A6-32
compile re-simulate command A6-13,

A6-34
compile-EPLD-netlist command A5-6
compile-error-check-ABEL-source command A5-3, A6-11, A6-33
compile-FPGA-netlist command A5-5
compile-FPGA-optimize command A5-5, A9-26
compile-options command A5-4, A5-7, A6-5, A6-11
compile-options dialog box A6-12, A6-27
compile-parse-ABEL-source command A5-4, A6-11, A6-16, A6-29, A6-31, A6-33
compile-parse-ABEL-vectors-only command A5-3, A6-11
compile-parse-vectors-only command A5-3, A6-34
compile-simulate-equations command A5-5, A6-12, A6-30, A6-34, A9-26, A9-37
compile-trace-options command A5-4, A6-13
compile-Xilinx-EPLD command A7-15, A7-16
compile-Xilinx-EPLD-netlist command A6-10, A6-33, A7-5, A7-17, A7-19, A7-20, A9-37
compile-Xilinx-EPLD-optimize command A5-6
compile-Xilinx-EPLD-options command A5-6, A6-10, A7-15, A7-16, A7-17
compile-Xilinx-FPGA-netlist command A6-7, A9-26, V14-10
compile-Xilinx-FPGA-optimize command A6-33, V14-10
compile-Xilinx-FPGA-options command A1-9, A1-10, A1-11, A5-5, A6-7
compiling designs E1-10, E3-9
complabels option V/ApD-15
complete option R2-190, R2-198, R2-217
COMPM L1-33, V5-11, V5-21
compnet option V/ApD-10
component attributes O5-16, V5-14
component availability, see Xilinx Libraries Guide for description and selection details
COMPONENT keyword E4-4, V5-13
components
  BUFFOE E4-12, E4-13
  choosing E4-9
  custom E4-1, E4-3
  device-specific F5-7
  enter O16-15
  GBUF E4-10
  IBUF E4-10
  label O16-21
  move O16-15
  OBUFEX1 E4-12, E4-13
  PL20 E4-2
  PL20V8 E4-2, E4-4
  PL22V10 E4-2, E4-4
  PL24 E4-2
  PL48 E4-2
  place O16-15
  PLFB9 E4-3
  PLFFB9 E4-3, E4-13
  XEPLD library, in schematics F5-3
composite block type V3-9, V5-12, V14-20, V/ApA-18
comptext V/ApD-10
concurrent loading U6-24
CONFIG attribute V4-8
  architectures L1-8
  purpose L1-8
  symbols L1-8
  syntax L1-9
  XC2000 CLB configuration options L1-9
  XC2000 IOB configuration options L1-9
  XC3000 CLB configuration options L1-10
  XC3000 IOB configuration options L1-10
CONFIG field O4-11

CONFIG property M4-10
config.sys file O2-4, V11-4, V11-5, V12-4
configuration U6-1
  data format U6-4
  data generation U6-1
  design directory O2-7
  Environment B3-4
  HDC U6-28
  LDC U6-28
  loading multiple devices U6-24
  modes U6-6
  OrCAD/ESP O2-6
  VST386+ O12-4, O12-18
    connectivity database extension O16-43
  XDM O11-69
  XEPLD environment O16-9
  XMake
    incremental design O11-98
configuration bitstream U7-1, U7-9
  XC3000 Demonstration Board H1-13
configuration command
  options
    donePad R2-246
configuration data U7-1, U7-11
  loading U6-21
configuration switches
  XC4000 Demonstration Board H2-11
configure U8-13, U8-17
configuring the XEPLD environment F/ApC-9
configuring your system M2-1
connecting 3V adapter
  XChecker H5-11
connectivity database extension O16-43
constraints
  APR R2-144
  PPR R2-185
  reading file in XDE R3-169
  reading schematic file in XDE R3-170
  setting file for CLBs/IOBs in XDE R3-146
  setting file for nets in XDE R3-146
  setting file for pins in XDE R3-146
  writing to file in XDE R3-194
constraints file R2-36, R2-37, R2-38, R2-39, R2-184, V11-10, V11-116
  BIDIR_IO B4-21
  example B3-18
  INPUTS B4-70
  OUTPUTS B4-82
constraints file *see* CST file L1-46
constraints flags O4-18
CONT field O4-11
context window V11-28, V16-15, V/ApA-23
conversion of PAL-based designs F2-26
conversion, *see* translation
converting designs M2-3
coordinates
  enabling X and Y O11-21
copy
  library symbols O11-38
copy command V11-49, V16-21, V/ApA-33
  XPP H4-20
Copy menu V/ApA-33
COUNT_TO attribute
  COUNTER B4-40
counter functions, see Xilinx Libraries Guide for description and selection details
COUNTER module B4-2, B4-36
  ASYNC_VAL B4-39
  BOUNDS B4-41
  cascading counters B4-45
  COUNT_TO B4-40
  ENCODING B4-41
  RLOC_ORIGIN B4-41, B4-112
  RLOC_RANGE B4-42
  STYLE
    BINARY B4-42, B4-43
    BINARY=Default B4-40

COUNTER module , STYLE *(Continued)*
Features B4-42
JOHNSON B4-40
LFSR B4-40, B4-43
ONE_HOT B4-44
SYNC_VAL B4-39
TNM B4-42
USE_RLOC B4-41
counters U3-10
COUT pin L1-100
COUT pin *see also* individual carry mode configuration mnemonics
COUT0 pin L1-100, L1-102
COUT1 pin L1-102
CRC U7-1, U7-15
during configuration U7-15
during readback U7-15
CRC configuration (XC4000 only) R2-248
create-new-PLD-and-PAL-interconnect-report command A7-18
CRF file R2-43, R2-45
XNFMAP R2-67
critical flag O4-18
critical net attribute *see* C net attribute
CRS file V/ApD-1, V/ApD-2, V/ApD-3, V/ApE-3, V/ApE-4
crystal oscillator R2-124, R2-239, R2-247, V9-4, V/ApF-7
XC3000 Demonstration Board H1-8
XC4000 Demonstration Board H2-1, H2-2, H2-12
CST file L1-46, R2-36, R2-37, R2-39
APR R2-133, R2-144, R2-145
BUFT constraints L1-67
CLB constraints L1-63
CLBMAP constraints L1-61
edge decoder constraints L1-69
flag constraints L1-52
flip-flop constraints L1-55
FMAP constraints L1-59
global buffer constraints L1-70
guided design R2-184
HMAP constraints L1-59
I/O constraints L1-64
input to PPR R2-174, R2-184, R2-185
IOB constraints L1-67
naming R2-190, R2-198, R2-217
Notplace Block constraints L1-49
Notplace Instance constraints L1-48, L1-54, L1-63, L1-67
Place Block constraints L1-49
place constraints L1-51
Place Instance constraints L1-48, L1-55
PPR L1-55, L1-67
RAM constraints L1-57
restrictions L1-54
ROM constraints L1-57
symbol names L1-54
syntactical conventions L1-50
syntax
conventions R2-220
restrictions R2-224
statements R2-222
wildcards R2-221
TIMEGRP constraints L1-54
TIMESPEC constraints L1-52
weight constraints L1-52
wildcards L1-50, L1-66
cstfile option R2-36, R2-37, R2-190, R2-198, R2-217, V11-148
CUPL F5-15, U2-3
see also PLD compilers
CUPL (PLD compiler) E1-3
current_state option A6-41, A6-44
cursor command F2-38
accessing through XDM R1-32
cursors R3-59, R3-85, R3-115
defining in XDM R1-32
selecting shape in XDelay R3-23
custom components E4-3
custom macros V5-12, V5-15

custom primitive symbols V5-4, V5-12, V5-15, V6-1, V6-7, V10-5, V10-8, V10-13, V16-47
CY4 primitives R1-117
CY4 symbol L1-72, L1-99, L1-100, R2-38, R2-42, R2-184, R2-191, R2-205, R2-207, V11-85
cycle command V/ApB-20
Cycle menu V/ApB-20
cyclic redundancy checking R2-230
cyclic redundancy checking *see* CRC

## D

D flip-flops A1-11, A7-14, A9-24, V14-7
D_IN
  COUNTER B4-37
  DATA_REG B4-49
  SRAM B4-106
D_OUT
  DECODE B4-59
  PROM B4-84
  SRAM B4-107
D1 input E5-28, E5-35
D2 input E5-28, E5-37
daisy chain R1-5, R2-252, R2-270, R2-273, R2-279, R3-65, U6-3, U6-5
  serial loading U6-23
  XChecker H5-48
  XPP H4-2
dangling nets V11-55, V11-112, V16-22, V/ApA-8, V/ApA-32, V/ApA-39
data
  directory F5-13
  feedback U3-9
  frames U6-5, U7-12
  readback output U7-8
data register U8-5
  cell U8-7
data register (DATA_REG) B4-48
data register functions, see Xilinx Libraries Guide for description and selection details
data type
  big–endian B2-18
  BOUNDS B2-16
  CAST B4-24
  COERCE B4-34
  ENCODING B2-16
  little–endian B2-18
  usage B2-16
data type propagation B2-21, B6-4
  usage B2-19
data values B2-6
  base B2-6
  binary B2-8
  decimal B2-8
  default B2-6
  dontcaredigits' B2-7
  format B2-8
  hexadecimal B2-8
  negative values B2-7, B2-18
  octal B2-8
  radix B2-6
  radix point B2-7
DATA_REG module B4-2, B4-48
  ASYNC_VAL B4-50
  BOUNDS B4-50
  ENCODING B4-50
  LOC B4-51
  RLOC_ORIGIN B4-51
  RLOC_RANGE B4-51
  STYLE attribute B4-52
  SYNC_VAL B4-50
  TNM B4-52
  USE_RLOC B4-51
DATA_REG symbol V13-10
database file F5-15
DATE keyword V16-29
date statement E2-2
DBA file O10-21
dc2p R1-89, V15-10
dc2p option R2-196, R2-198, R2-218

dc2s R1-86, V15-10
  overlapping specifications R1-87
dc2s option R2-196, R2-199, R2-218
DCSET directive A3-7, A9-21, A9-25
DCSTATE directive A3-7, A4-17, A6-9, A6-25
DDP M2-2
debug
  functional simulation O12-23
debugging
  all families U6-46
  daisy-chain configurations U6-55
  design verification U6-45
  failed configuration U6-49
  general U6-45
  hints U6-45
  incorrect configuration U6-49
  Master Parallel Up/Down Mode U6-49
  Master Serial Mode U6-50
  Peripheral Mode U6-51
  Slave Mode U6-53
  XC2000 devices U6-47
  XC3000 devices U6-47
  XC4000 devices U6-48
DEC-F-CI L1-114
DEC-FG-0 L1-117
DEC-FG-CI L1-115
DEC-G-0 L1-115
DEC-G-CI L1-116
DEC-G-F1 L1-116
DEC-G-F3- L1-117
decimal B2-8
declarations section (PLUSASM) E2-3
declarations statement A7-4, A9-24
DECODE attribute L1-69, O4-14, V4-4
  architectures L1-11
  purpose L1-11
  symbols L1-11
  syntax L1-11
decode logic L1-28
DECODE macro L1-69
DECODE module B4-2, B4-58
  Select warning message B4-58
DECODE property M4-4
DECODEMASK attribute B2-9
DECODEn symbols L1-20
decoder functions, see Xilinx Libraries Guide for description and selection details
decoders L1-72
  edge A1-13
DEF attribute A5-10, O4-14, R1-113, R1-118, V13-9, V14-15
DEF=PLD M5-14
default clock
  PLFFB9 E4-13
default options, selecting F2-39
default timing specifications R1-72
default.dvpt M6-7
defining a function key F2-38
delay
  specifying via XACT–Performance R1-69
delay option M8-5
delay paths
  ending at clock pins R3-13
  ending at clocked elements R3-9
  order displayed in XDelay R3-14
  starting at clocked outputs R3-10
  starting at clocked outputs, ending at clocked inputs R3-10
delete command V11-58, V11-141, V16-17, V16-48, V/ApA-32
Delete menu V/ApA-32
deletenet option V/ApD-15
deleting extra files F2-34
DeMorgan equivalent functions E2-14
demultiplexer functions, see Xilinx Libraries Guide for description and selection details
DEPTH attribute
  PROM B4-85

SRAM B4-107
design L1-94
behavioral F/ApC-11
choosing target device F2-17, F2-40
compiling E3-9
creation B3-3
design check O11-67
design directory creation O2-6
design entry tutorial O11-1
design example B3-15
design flow B6-1
design process B3-1
downloading B3-14
downloading to an FPGA O11-91
example F/ApC-2
equation files F/ApC-12
functional simulation B3-8
implementation B3-10
FPGA O7-3
incremental design O11-95
incremental flow B3-2
optimization E5-22
overview of procedure F1-1, F5-1
PLUSASM
annotation statements F4-4
testing the design O11-92
timing simulation B3-12
verification E5-5
design architect , see also PLD_DA
design architect M1-1
tutorial
.PRO files M11-83
adding buses M11-35
adding labels M11-56
adding nets M11-36
adding pins to symbol M11-22
adding ports M11-42
adding text M11-25
assigning pin locations M11-69
bus rippers M11-45
calc_3k M11-9
checking design rules M11-96
checking for errors M11-109
command summary M11-111
completing ALU schematic M11-50
configuring system M11-5
configuring XMake with XDM M11-80
constraints file M11-81
copying components M11-33
copying files M11-13
creating ANDBLK2 symbol M11-21
creating ORBLK2 symbol M11-28
creating schematics for symbols M11-30
demonstration board M11-97
design description M11-19
download cable M11-97
downloading bitstream M11-101
entering commands M11-18
examining routed design M11-93
FAST pads M11-71
FD4CE symbol M11-54
files used M11-8
finding block M11-95
guide file M11-106
highlighting net M11-96
I/O flip-flops M11-72
incremental changes M11-105
installing M11-7
inverting output display signals M11-67
labeling buses M11-44
labeling nets/buses M11-39
Men2XNF8 M11-83
Mentor graphics variables M11-6
net connections M11-38
opening calc schematic M11-63
optimizing for XC4000 M11-73
placing library components M11-53

design architect *(Continued)*
placing user-created components M11-51
PLD_XMake M11-85
RAM stack M11-75
required software M11-5
saving ALU schematic M11-58
saving calc schematic M11-73
saving symbol M11-27
schematic layout M11-69
solution files M11-8
stack implementation M11-74
state machine M11-77
targeting for XC4000 M11-14
testing design M11-103
translating design M11-108
using function keys M11-17
using mouse M11-16
viewing primitive M11-60
viewing RPM M11-61
viewing soft macro M11-59
wide-edge decoders M11-78
XC3000 demo board M11-101
XC3000 oscillator M11-64
XC3000/XC4000 demo board M11-99
XC4000 demo board M11-100
XC4000 oscillator M11-65
Xilinx library elements M11-58
design DataPort M2-2
Design Editor, see XDE
design entry U1-13, U2-1
Boolean expressions R1-2
controlling implementation U2-4
library elements U2-1
schematic entry U2-1
schematics R1-2
state expressions R1-2
text–based entry U2-3
Design Entry & Conversion
programs in R1-3
Design Entry menu F2-18, R1-19
design file, creating
creating a design directory O2-6
entering the Draft editor O2-15
hierarchical symbols
sheet path part O3-7
sheet symbol O3-6
naming conventions O3-1
naming nets and subnets O3-2
schematic O11-37, O16-10, O16-14
design flow M1-1, M11-2, O1-1, R1-2, U1-13
design entry U1-13
design implementation U1-13, U5-1
design verification U1-13
functional simulation O10-11
implementation (EPLD) O7-8
timing simulation (EPLD) O10-19
timing simulation (FPGA) O10-17
XNF file creation O10-3
design hierarchy L1-16, L1-17, L1-45, L1-75, L1-76, L1-78, L1-79, L1-80, L1-82, L1-92
design implementation U1-13, U3-1
bitstream creation R1-2
bitstream generation U3-7
mapping R1-2, U3-5
merging U3-5
optimization U3-4
placement R1-2, U3-6
programs in R1-4
routing R1-2, U3-7
XNF translation U3-3
design implementation flow U5-1
XC2000 U5-1
XC2000L U5-1
XC3000 U5-1
XC3000A U5-3
XC3000L U5-3
XC3100 U5-1
XC3100A U5-3
XC4000 U5-4
XC4000A U5-4

XC4000H U5-4
design issues
EPLD devices O3-1, O5-1
FPGA devices O3-1, O4-1
Design Manager A1-6, M1-1
defining the interface M1-3
Icons M1-3
see also XDM, PLD_XDM, PLD_DMGR
design performance U3-7
design process
tasks O1-2
design rule checker integrator module F5-7
Design Rule Checker, *see* DRC
design rule checking M7-8, M11-96, R2-29, R2-227
design size U3-7
estimating U3-8
design verification U1-13, U6-45
functional simulation U4-4
in-circuit verification R1-3
programs in R1-5
simulation R1-3, U4-3
static timing analysis R1-3
timing simulation U4-4
XChecker program O11-86
Design Viewpoint Editor
see PLD_DVE
design.out file M7-2
design-design command V15-30
DesignEntry menu V2-13, V11-16, V11-140, V12-33, V16-11
DesignEntry SYMGEN command V14-11
DesignEntry Workview command V2-3, V2-13, V11-15, V12-33, V12-52, V16-11, V16-39
DesignEntry XABEL command A5-1, V14-4
detailed option A6-29
detailed trace option A6-14
DEV file
APR R2-144
device
basic structures E2-4
choosing target for design F2-17, F2-40
determining speed of F2-40
family selection E1-6, E3-7
part type selection E1-6
pin assignment E5-1
programming E1-11, E3-9, E4-9
speed selection E1-7, E3-7
XC7000 F/ApC-9, F/ApC-10
XC7200 and XC7300 F2-17
DEVICE attribute V15-12
device polarity A4-5, A6-11, A6-27, A7-14, A7-15, A/ApB-1, A/ApB-2
device statement A7-5, A7-19, A9-34, A/ApB-2
device-independent designs A9-33
device-specific designs A9-33
DFF L1-72, V/ApE-2
dflt_sig_dly option R2-197, R2-200, R2-218
dialog boxes A2-3
dialog-box command V/ApA-2, V/ApA-8, V/ApA-26, V/ApA-31, V/ApA-39
DIN pin V9-2
DIP switches V11-134
XC3000 Demonstration Board H1-4, H1-6, H1-12
XC4000 Demonstration Board H2-1, H2-2, H2-9
DIR keyword V2-4, V2-6, V11-8, V11-14, V/ApD-6, V/ApF-1, V/ApF-2, V/ApF-3, V/ApF-5, V/ApF-6
DirClean command F2-34
XDM R1-30
direct inputs E2-8
direct interconnect U1-10, U9-28
direct outputs E2-18
directories
CLIB F5-13
data F5-13

directories *(Continued)*
design directory creation O2-6
design_tim B3-12
MSG F5-13
otherxnf B3-8, B3-12
sdesign B3-8, B3-12
selecting current directory F2-34
simdir B3-8
structure O2-2
structure of, in XDM F5-10
tutorial F5-13, F/ApC-9, F/ApC-10
viewing structure F2-34
XACT root directory F5-13, F/ApC-5
directory command F2-34, F/ApC-9, F/ApC-10
XDM R1-30
directory settings field F2-17, F/ApC-9, F/ApC-10
Display Manager F2-4, R1-12
Display menu
ViewSim V/ApB-12
ViewWave V/ApC-24
display-change command V/ApB-12
display-info command V/ApB-14
display-inputs command V/ApB-12
display-path command V/ApB-13
display-stats command V/ApB-13
display-xhair-off command V/ApC-24
display-xhair-on command V/ApC-24
DIVIDE_BY attribute
CLK_DIV B4-30
divider integrator module F5-9
DMC file A1-8
do file M9-1
documentation
design implementation U3-3
interface user guides U1-17
XACT Hardware and Peripherals Guide U1-17
XACT Libraries Guide U1-16
XACT Reference Guide, Volume 1 U1-16
XACT Reference Guide, Volume 2 U1-17
XACT Reference Guide, Volume 3 U1-17
XACT User Guide U1-16
X-BLOX User Guide U1-16
Xilinx ABEL User Guide U1-16
don't-care digits B2-7
don't-care option A6-9, A6-25, A6-41, A6-44
don't-care simulation values A6-14, A6-30, A6-49
don't-care X-value option A6-30
DONE U8-9
DONE alignment U6-41
DONE pin pullup
XC3000 R2-247
XC4000 R2-248
DONE timing
XC3000 R2-247
DOS A6-3, R3-21, V1-1, V11-3, V11-119, V11-125, V12-3, V12-31, V12-50, V14-10, V14-17, V16-5, V16-10, V16-28
accessing through XDM R1-30
DOS command
entering from within XDM F2-35
XDM R1-30
dot extensions A7-2
.ap A7-12
.ar A7-12
.ce A7-14
.d A4-8
.fb A7-12
.pin A7-12
.q A7-12
asynchronous latches A1-12
attributes A4-6, A4-7, A7-14
buried-node numbers A4-16, A7-20, A8-2
device support A/ApB-1

dot extensions *(Continued)*
EPLDs A7-11, A7-12
FPGAs A4-8
JK flip-flops A4-13
listing-with-index command A6-18
macrocells A6-14, A6-29, A6-49
purpose A4-8
Set-Reset flip-flops A4-15
signal names A6-30
toggle flip-flops A4-14
unsupported A7-13
XC2000 family A4-9, A4-12, A4-13, A4-14, A4-15
XC3000 family A4-10, A4-13, A4-14, A4-15
XC4000 family A4-11, A4-13, A4-14, A4-15
DOUBLE attribute O4-14, V4-4
architectures L1-11
purpose L1-11
symbols L1-12
syntax L1-12
DOUBLE property M4-4
download cable U1-13, V11-131
in slave-serial mode U6-20
usage U4-9
using BIT file U6-3
XC4000 V11-135, V11-136, V11-146
downloading hex files F2-33
downloading process U6-1
downloading the design
XChecker O11-91
DP V3-2
dp2p R1-90, V15-10
dp2p option R2-196, R2-200, R2-219
dp2s R1-88, V15-10
dp2s option R2-201, R2-219
draft
EPLD designs
tasks O16-10
Draft Edit menu, *see* Edit menu
draw
buses O11-40
wires O11-40
DRC M11-96, R2-227, U3-7, U4-9, V7-6, V11-129, V14-22
EditLCA program O11-85
XNFPrep output O11-75
DRCK U8-10
DS120 programmer F/ApC-22
dummy arguments A6-44
dumpm command V/ApB-23
DUTY_CYCLE attribute
CLK_DIV B4-30
dw option V10-14

## E

edge decoders A1-13, L1-11, L1-46
constraints L1-69
edge designations L1-69
edge location
ANDBUS location attribute B4-3
EDIF V7-7
EDIF file M10-7, M10-22
EDIF primitive library M10-19
EDIF2XNF M10-5, M10-7, M10-8, M10-11, M10-18
error messages M/Ap-1
options M10-19
signal naming conventions M3-3
symbol naming conventions M3-3
syntax M10-19
variables M10-19
edit command A6-4, A6-23, F2-35, F3-1, O16-9
accessing through XDM R1-30
stimulus file O16-50
Edit menu V/ApC-17
PCs A6-3
workstations A6-21
XC2000/XC3000 field names
BASE and CONFIG O4-11

Edit menu *(Continued)*
BLKNM O4-11
EQUATE and CONT O4-11
LOC,OPTIONS O4-10
XC4000 field names
BASE and CONFIG O4-12
EQUATE O4-12
INIT O4-12
OPTIONS_1 O4-12
OPTIONS_2 O4-12
edit modes
safe, expert R3-66
EditBlk screen U9-10
edit-clear command A6-22
edit-copy command A6-22, V/ApC-20
edit-cut command A6-22, V/ApC-20
edit-delete command A6-22
edit-delete-line command A6-4
edit-edit command A5-3
edit-find command A6-22
edit-go-to command A6-22
editing files F2-35
editing window A2-1, A6-22
edit-insert command V/ApC-17
EditLCA H1-13, L1-6, L1-26, L1-65, O15-48, O15-49, R2-241, U6-2, V11-125, V11-126, V11-129, V11-130, V15-30, V15-42, V15-43
EditLCA Screen U9-5
editlca.pro file R3-68, R3-170, R3-176
edit-next command A6-4
edit-off command V/ApC-19
editor environment variable F/ApC-5, V16-6
editor icon M1-5
editor-options dialog box A6-32
edit-paste command A6-22, V/ApC-21
edit-repeat command V/ApC-19
edit-replace command A6-22, V/ApC-18
edit-replicate-line command A6-4
edit-search command A6-4
edit-subst command V/ApC-21
edit-tlimit command V/ApC-22
edit-tstep command V/ApC-22
edit-undo command A6-22
electrical rule check V11-1
ELEM attribute
ELEMENT B4-60
ELEM port
ELEMENT B4-60
ELEMENT module B4-2, B4-60
ELEM B4-60
EN
CLK_DIV B4-29
enable-auto-make option A6-31
encode option A6-38, A6-42
encoded state machines A3-5
example A3-13, A9-28
encoder functions, see Xilinx Libraries Guide for description and selection details
ENCODING attribute B2-16, V13-8, V13-9
BIDIR_IO B4-19
BIT B2-17
BUS_DEF B4-22
CAST B4-27
COUNTER B4-41
data type propagation B2-19
DATA_REG B4-50
FORCE B4-62
INPUTS B4-69
one_hot B2-17
OUTPUTS B4-81
PROM B4-85
SHIFT B4-97
SRAM B4-108
TWO_COMP B2-17
UBIN B2-17
usage B2-16
encoding option A6-9, A6-25
encoding techniques A1-9, A3-4, A6-9, A6-25, A6-38, A6-42

end statement A3-10, A3-13, A3-15, A3-19, A9-21, A9-25, V14-10
Enprtsc key R3-131
environment variables
  editor F/ApC-5
  XACT F/ApC-5
environment, configuring F/ApC-9
ENWRITE M10-22
  EDIF2XNF M10-19
  functional simulation M10-5, M10-7, M10-8, M10-11
  options M10-22
  REF property M4-1
  syntax M10-22
  variables M10-22
EPLD, see also EPLD designs and EPLDs
EPLD M5-1
  3-State multiplexing M5-7
  BUFG M5-7
  clocks M5-7
  components M5-1, M5-8
    counters M5-11
    PLD M5-12
  FastCLK M5-7
  FOE line M5-3
  functional simulation M6-2, M9-5, M10-2
  global control nets M5-7
  input/output buffer connections M5-2
  output buffers and 3-States M5-3
  primitives and macros M5-13
  XC7000 library M5-1
EPLD designs
  3-State buffers O5-4
  3-State multiplexing O5-7
  arithmetic components O5-11
  bidirectional I/O pin O5-5
  buffers O5-2
  counters O5-11
  design issues O3-1, O5-1
  device initialization
    functional simulation O9-5
    timing simulation O9-5
  EPLD-specific components O5-9, O5-10
  fast output enable O5-2
  fitting the design O16-35
  functional simulation O6-1, O9-6
  High-Z O9-6
  input buffers O5-2
  library components O5-1
  macros O5-13
  output buffers O5-4
  pads O5-2
  PLD components O5-11
  PLUSASM equations O5-13
  power and ground signals O5-14
  primitives O5-13
  timing simulation O8-1, O9-5
  user-defined macros O5-13
  user-defined primitives O5-13
EPLDs U1-1
  3-state buffers V5-3
  3-state multiplexing V5-6
  ABEL-HDL file structure A7-2
  area and speed optimization A1-13
  attributes A6-11, A6-27, A7-13
  bidirectional I/O pins V5-3, V5-5
  buffers V5-1
  component attributes V5-15
  components V5-1
  converting ABL file to PLUSASM A7-17
  converting equation files to XNF format V3-9
  converting JEDEC files A8-1
  custom macros *see* custom macros
  custom primitive symbols *see* custom primitive symbols
  design flow A1-1, V1-4
  designs supported A1-1, A1-9, A1-12

EPLDs *(Continued)*
- device architectural features A7-1, A7-9
- devices supported V1-3
- dot extensions A7-11, A7-12, A7-13
- encoding compromises A3-5
- encoding techniques A1-13, A3-6, A3-7
- equations report A7-22, A7-23
- example A9-36
- files processed in design flow A1-4
- fitter A7-4, A7-5, V5-3, V5-17, V5-20, V16-22, V16-23, V16-32, V16-33, V16-34, V16-35, V16-37
- functional simulation *see* functional simulation
- general-message-log report A7-22, A7-23
- global attributes V5-17
- implementing designs V1-4, V7-1, V7-7, V10-13, V16-34
- incompletely-specified state machines A1-13
- input buffers V5-2
- library search order V2-8
- logic-optimization and device-assignment report A7-22
- macros V5-12
- mapping report A7-22
- minimization A6-11, A6-27, A7-14
- multiple-source files A7-3, A7-4, A7-17
- one-hot encoding A3-6
- optimization by BLIFOPTX A1-6
- optimize options A6-11, A6-26
- output buffers V5-3
- pads V5-2
- partition-log report A7-22
- pinlist report A7-22
- PLD symbols *see* PLD symbols
- PLUSASM-assembly-log report A7-22, A7-23
- polarity A6-11, A6-27, A7-15
- power and ground signals V5-13
- primitives V5-12
- PRLD signal V9-5, V9-8, V16-41
- resource report A7-22
- signal saving A1-11
- simulating V9-5, V16-41, V16-54
- source file example A7-10
- source files A7-1
- state-machine synthesis A5-6
- timing simulation *see* timing simulation
- timing specifications A1-13
- unsupported features A1-12
- XEMake A1-12
- Xilinx ABEL design flow A1-4
- Xilinx Property-Initialstate keyword A3-11
- XOR gates A7-16
- XSimMake A1-12

EPROM R2-238, U1-13, U6-8
EQN M6-5, M8-3, M10-5
EQN file A5-7, A6-6, A6-35, A7-23, E5-5, F3-33
EQN symbols R3-30
equate field O4-11
EQUATE_F attribute V4-8
- architectures L1-12
- purpose L1-12
- syntax L1-12

EQUATE_F property M4-10
EQUATE_G attribute V4-8
- architectures L1-12
- purpose L1-12
- syntax L1-12

EQUATE_G property M4-10
equation files V1-4, V3-9, V5-1, V5-4, V5-10, V5-12, V5-13, V5-14, V5-15, V5-18, V7-1, V10-5, V16-3, V16-10, V16-15, V16-29, V16-34
- assembling F2-22
- examples F/ApC-12

equations A1-6, A4-5, A4-17, A6-6, A6-12, A6-36, A6-38, A7-23
ADD F4-44
ADDMODE F4-46
ALU format F4-40, F4-41
chaining across FB boundaries E5-3
CLKF F4-48
collapsing E5-5
combinational E2-12, E2-15
combinatorial and registered F4-40
control F4-43
defining signal polarity F4-66
EXPORT F4-52
FBK F4-54
FI F4-56
for example design F/ApC-12
keyword E2-4
linked E5-3
manual partitioning E2-16
PIN F4-57
PRLD F4-58
registered E2-10, E2-15, E3-18
RSTF F4-48, F4-59
section (PLUSASM) E2-4
SETF F4-48, F4-60
SHIFT F4-61
splitting E4-2, E5-8, E5-13
splitting effects E5-15
TRST F4-65
EQUATIONS keyword V16-29
equations report A7-22, A7-23, E5-5, E5-8
equations statement A3-11, A3-17, A4-17, A7-9, A9-21, V14-8
ERC O16-35
err file F5-1, F5-16
err output R1-66
err.err file A1-8, A5-3, A6-6, A6-36, A6-42, A6-45, A6-46
errlog option A6-42, A6-45, A6-46
error messages
ABL2XNF A/ApA-1
AHDL2X A6-36, A/ApA-2
ImproveX A6-6, A6-36, A/ApA-11
Mentor M/Ap-1
SDT2XNF O/ApB-2
StateX A6-6, A6-36, A/ApA-2
SynthX A6-6, A6-35, A/ApA-12
XChecker H5-60
XDraft O/ApB-1
XNF2VST O/ApB-5
XPP H4-27
errors F5-16
erxport-wirelist-Viewsim command V10-8
ESP design environment
software installation O2-2
estimate option R2-189, R2-202, R2-217
every command V/ApB-23
EXAMINE-CI L1-100, L1-122
example design F/ApC-2
example files F/ApC-4
ABEL F/ApC-11
examples directory B1-2
EXCEPT statement V15-7, V15-9
EXCEPT statement, *see* XACT-performance
exe files F5-13
executable files F5-13, R1-8
execute command
accessing through XDM R1-31
Execute menu V/ApB-20
execute-cmdfile command V/ApB-20
execute-logfile command V/ApB-21
exit
SDT O11-68, O16-29
VST O12-25, O16-61
XDM O11-101, O16-61
exit command A7-19
exiting
temporarily, to DOS F2-35
XDM F2-3, F/ApC-6
EXORMAX format R2-270, R2-271, R2-274, R2-278, R2-281

XPP H4-2
expanded option A6-27, A6-39
expanded-listing option A6-12
explicit (X) attribute R2-60
export
block O11-41
export-check command V/ApA-27
EXPORT equation F4-52
Export menu V/ApA-26
export-check command V/ApA-16
export-wirelist-Viewsim command V6-7, V10-8, V12-9, V12-32, V16-54, V/ApA-26
EXT attribute V11-96
EXT records L1-64, M10-20
external (X) flag O4-19
external I/O attribute O4-4, O4-13
external IOB R2-146
external net attribute *see* X net attribute
Extest U8-3, U8-6, U8-7, U8-13, U8-15
data flow U8-15

## F

F attribute M5-22
F mode L1-2
F net attribute L1-33, V5-20
F schematic attribute E4-12
factoring A3-5
FailedSpec option V15-28, V15-33
FailedSpec XDelay option O15-39
FALLING R1-79
family command F2-38
accessing through XDM R1-32
family option A6-8, A6-24, A6-39, A6-43
family settings field F2-17, F/ApC-9, F/ApC-10
FAST attribute O4-14, O11-57, V4-7, V11-99, V/ApE-2
architectures L1-13
purpose L1-13
symbols L1-13
syntax L1-13
fast function blocks L1-33, L1-38, V5-20
fast inputs E5-9
fast output enable (FOE) O5-2, V5-3, V5-11, V5-18, V5-21, V/ApD-5
Fast Output Enable see FOE
FAST property M4-8
FAST3KA attribute B4-12, B4-16, B4-66, B5-3
fast-carry logic A1-13
FastCLK L1-39, M5-7, M5-21, V5-18, V5-19, V16-18
design rules F5-8
input, assigning O16-17
nets E2-16, E3-4, E3-17, E4-9, E5-26
optimization L1-7
pin F4-10
FASTCLOCK statement E3-4, F4-10
fast-function blocks (FFB) E2-4, E2-15
assigning equations E3-18
attribute O5-24
exporting product terms E5-26
partitioning E5-26
FastInput (FI)
path L1-33
pins F4-12, F4-56
source equation F4-56
statement E4-13, F4-12
fast-output-enable signals A7-7, A7-8, A7-22
FB (high-density function block) E2-4
FBK equation F4-54
FD registers L1-39
FD4CE V11-69, V11-71, V11-78
FDCE L1-5, L1-72
FDCP L1-5, L1-33, V5-11, V5-21
FDCPE L1-33, V5-11, V5-21
FDPE L1-5, L1-72
FDR flip-flops V9-2, V12-18
FDS flip-flops V9-2, V12-18
FFB L1-33
FFB product term assignment equation

(EXPORT) F4-52
FFS set V15-6, V15-7, V15-8, V15-11, V15-14, V15-15, V15-17, V15-19
FG mode L1-2
FGM mode L1-2
FI equation F4-56
FI modifier (fast input) E3-18
Fibonacci sequence B3-15
field names
XC2000, XC3000 O2-10
XC4000 O2-10
Field Programmable Gate Array *see* FPGA
fields
settings F2-17
FIFO B4-92
file.blx B2-23
FILE attribute A5-10, O4-15, V1-4, V3-10, V3-11, V4-3, V6-3, V6-7, V6-8, V12-29, V14-15, V14-21, V/ApE-3
architectures L1-13
example L1-14
purpose L1-13
syntax L1-14
File menu
PCs A6-1
ViewDraw V/ApA-16
ViewWave V/ApC-11
workstations A6-19
FILE property M4-2, M6-5, M10-3
functional simulation M10-8, M10-11
timing simulation M10-15
file-dir-memory command V/ApA-17
file-dir-schematic command V/ApA-18
file-dir-symbol command V/ApA-18
file-DOS-shell command A6-3
file-exit command A5-3, A5-9, A6-3, A6-21, V14-10, V14-11
file-insert command A5-3, A6-2, A6-20
file-new command A5-2, A6-1, A6-20
file-open command A5-2, A5-3, A6-2, A6-20
file-print command A5-3, A6-3, A6-21
file-read command V16-47, V16-50, V/ApA-17
file-read-savefile command V/ApC-12
file-restore command V/ApA-19
files
*see also* macro files
.bat F5-13
ABEL examples F/ApC-11
ABL file O16-33
AST file O6-4, O8-4, O10-20
ATR file O6-4, O8-4, O10-20
database F5-15
DBA file O10-21
deleting extra F2-34
directories F5-10
editing F2-35
equation, assembling F2-22
err F5-1, F5-16
exe F5-13
functional netlist creation O6-1
guide O11-95
hex F5-16, F/ApC-22, O10-21
creating F2-32
downloading F2-33
INF O10-5
JEDEC F5-15, F5-16
creating F2-31
LCA file O7-1, O7-11, O10-15
log F5-1, F5-16
MAP F/ApC-21
netlist F5-3, F5-15
NRF O10-20, O10-21, O12-14
PAR F/ApC-22
PDS F5-15
pin F/ApC-21, O16-39
PLD F5-15, O16-32
PLUSASM equation F5-15
PPR
log file O15-30
PRG F/ApC-22, F5-16

files *(Continued)*
PROGLIST.XDM F2-1
program list F2-1
programming F5-16, F/ApC-22
PRP file O11-76
RCVR.ABL F/ApC-14, O16-33
RCVR.PDS F/ApC-12
report F5-15, F/ApC-21
RES F/ApC-21
sdt.cfg O2-10, O11-6
STM file O12-17, O16-45, O16-50
timing netlist creation O8-1
TRC file O12-17, O16-47
tutorial example F/ApC-4
TXT F5-13
UART_EQN.PLD F/ApC-17, F/ApC-18
viewing F2-34, F2-35
VMF F2-18, F2-23, F/ApC-20, F/ApC-22
VMF O16-40
VMH O7-1, O7-12, O16-37
VMH or VMD F5-15
VST F2-29, F/ApC-23, O10-16, O10-20
vst.cfg file O2-12, O12-3
WIR F/ApC-23
wirelist F2-30, F2-31, F2-32
XDM.PRO
reading F2-40
writing F2-40
XEPLD.CFG F5-13
Xsimmake.out file O12-13
file-save command A5-3, A6-2, A6-20, V/ApA-40
file-save-and-exit command A6-3
file-save-as command A5-3, A6-2, A6-20
file-savelog command V/ApA-19
file-save-options command A6-2, A6-21
file-write command V3-9, V11-41, V11-51, V11-66, V11-76, V11-100, V11-103, V11-106, V11-110, V11-111, V11-112, V11-142, V13-9, V14-13, V15-12, V15-16, V15-18, V15-20, V16-28, V/ApA-16
file-write-cmdfile command V9-9, V12-35, V16-40, V/ApC-11
file-write-savefile command V9-9, V12-28, V/ApC-12
file-writeto command V11-43, V11-52, V11-65, V11-77, V11-83, V16-28, V16-47, V16-48, V16-50, V/ApA-16
first-display-vector option A6-15
first-vector option A6-30
FITEQN
accessing through XDM R1-25
FITEQN command F2-24, V7-1, V10-16, V10-22
example F/ApC-20
FITEQN menu
command E1-10, E3-9, E5-4, E5-5
FITNET M10-13
accessing through XDM R1-25
FITNET command A7-19, A7-21, F2-25, F5-3, L1-37, V7-7
driving unused components to GND V/ApD-5
ignoring pin assignments V/ApD-5
implementing device V5-14, V7-1, V7-10, V10-13, V10-16, V16-34
integrating PLDs into device V5-10, V5-15, V7-12
options
-f V16-37
-i V/ApD-5
-u V/ApD-5
output V10-22
purpose V7-1
reports V16-35
running with XEMake V7-10
FITNET menu
command E4-8
FITNET program O10-15, O16-35
reports O16-39

fitter M3-8
error report V16-35
invoking F/ApC-20, O16-36
results (report) F3-2
fitter fiteqn command A5-9, A7-4, A7-7, A7-17, A7-18, A7-21, A9-37
Fitter FITNET command *see* FITNET command
fitter general-log file V16-35
Fitter menu F2-24, R1-24
command E3-9, E5-4
fitter palconvt command A7-18
fitting strategies E5-22
fixed-polarity option A6-11, A6-27, A7-16
flag constraints L1-52
flag IOB constraint R2-149
flag net constraint R2-149
flagblk option V15-28, V15-30, V15-34
flagblk XDelay option O15-36
flat designs O3-3
flatten option V/ApD-10
flattened files R2-1
flip-flop functions, see Xilinx Libraries Guide for description and selection details
flip-flops L1-5, M9-2
asserting global reset signal V9-1, V12-17
asserting global set/reset signal V9-2, V12-18
BLKNM attribute V4-3
CLB V4-9, V9-3
clock pins L1-33
constraints L1-55
CST file L1-55
D A1-11, A7-14, A9-24, V14-7
ending points for path delay in XDelay R3-6
FDR V9-2, V12-18
FDS V9-2, V12-18
grouping into FFS set V15-6
grouping with EXCEPT statement V15-7
grouping with TIMEGRP symbol attributes V15-7
hold violations V9-2
I/O O11-58, V4-9, V11-101
initializing V9-1, V12-18
inputs A1-13, V15-29
IOB A1-13, L1-35, V15-14
JK A1-11, A4-13, A7-14
LOC constraint V4-5
macros L1-93
merging into IOBs B6-4
NODELAY attribute V4-7
optimization F5-9
outputs A1-13, V15-29, V15-38
path delay V15-9, V15-30, V15-40, V15-41
Q output L1-2
reducing logic levels on critical paths V15-10
reset signal V11-91
set-reset A4-15
dot extensions A4-15
setup times V15-29
SR A1-11, A7-14
stack V11-29, V11-104, V15-15
starting points for path delay in XDelay R3-6
state machine V11-107, V14-7, V15-17
T A1-11, A7-1
TNM attribute V15-4, V15-5
toggle A4-14, A7-14
dot extensions A4-14
use with BLKNM attribute L1-5
use with FAST attribute L1-13
use with LOC constraint L1-19, L1-24, L1-55
use with RLOC constraint L1-73, L1-78, L1-81
X L1-25

flip-flops *(Continued)*
XC3000A/L L1-55
XC4000 primitives L1-5
Y L1-25
FLOAT_HMINPUT string R1-112
FLOAT_VAL attribute
BIDIR_IO B4-20
example B2-12
INPUTS B4-69
OUTPUTS B4-81
TRISTATE B4-111
usage B2-12
floorplanning V15-10
flying lead connectors
XC4000 Demonstration Board H2-6
XChecker H5-13
FMAP V4-3, V4-4, V4-5, V11-85, V15-10
constraints A1-10, L1-59
mapping constraints L1-59
placement constraints L1-46
relationally placed macros L1-96
schematics example L1-60
symbols R2-184, R2-191, R2-205, R2-217, U2-4
unified libraries L1-72
use with BLKNM attribute L1-5
use with HBLKNM attribute L1-16
use with LOC constraint L1-19, L1-20
use with MAP attribute L1-29
use with net attributes L1-34
use with Place Block constraint L1-49
use with RLOC constraint L1-72
FNCSIM8 M6-4
manual translation M10-1
options M10-23
see also functional simulation
see also PLD_FNCSIM8
syntax M10-22
variables M10-23
fncsim8.log M6-6
fncsim8.sh M6-6
FOE L1-15, L1-33, O5-2
design rules F5-8
pin option F4-19, F4-30
pins F4-13
FOE modifier E2-17
FOE nets E2-16, E3-4, E3-17, E3-18, E4-12, E4-13, E5-26
FOE signals A7-7
FOE_OPT attribute O5-22, V5-18
architectures L1-15
purpose L1-15
syntax L1-15
FOE_OPT property M5-16, M5-21
FOEPIN statement E2-11, E2-17, E3-4, E3-17, F4-13
footprints V1-3
Force menu V/ApB-16
FORCE module B4-62
BOUNDS B4-62
ENCODING B4-62
VALUE B4-63
FORCE-0 L1-121
FORCE-1 L1-121
FORCE-CI L1-121
forced_on setting R2-192, R2-215
FORCE-F1 L1-121
FORCE-F3 L1-122
force-H command V/ApB-16
force-L command V/ApB-16
force-X command V/ApB-17
forward tracing R1-93, V15-5
TS flags R1-96
FPGA
advantages U1-1
architecture U1-2
area and speed optimization A1-9
attributes A4-5
bidirectional pins A1-12
configuration data U1-2
converting JEDEC files A8-1
design flow A1-1, U1-13

FPGA *(Continued)*
design issues O3-1, O4-1
designs supported A1-1, A1-9
dot extensions A4-8
edge decoders A1-13
encoding compromises A3-5
encoding techniques A3-6
families U1-2
fast-carry logic A1-13
files processed in design flow A1-2
I/O pads A1-13
incompletely-specified state machines A1-11
input flip-flops A1-13
IOB flip-flops A1-13
IOB three-state buffers A1-13
libraries O4-2
logic-level specifications A1-10
mapping A1-10
minimization A6-8, A6-24
one-hot encoding A3-6
optimization by BLIFOPTX A1-6
output flip-flops A1-13
place-and-route constraints A1-12
primitives and macros O4-2
RAMs A1-13
ROMs A1-13
signal saving A1-11
standard encoding A3-7
state-machine speed-optimization A1-11
state-machine synthesis A5-5
unsupported features A1-12
Xilinx ABEL design flow A1-2
XMake A1-12
XSimMake A1-12
FPGA Demonstration Board V11-88, V11-92, V11-130, V11-131, V11-133
+5V Power Connector H3-7
+5V Regulator Option H3-7
7-Segment Displays H3-9
Crystal Oscillator H3-12
downloading with XChecker H3-25
Eight General-Purpose Input Switches H3-8
example H3-27
features of H3-1
general components H3-7
I/O connections H3-11
Jumper J7 H3-15
LED Indicators H3-10
loading with configuration PROM H3-26
Mode switch settings H3-20
operation H3-25
PROGram Pushbutton H3-8
Prototype area H3-12
purpose H3-1
Relaxation Oscillator components H3-19
RESET Pushbutton H3-8
Serial PROM Socket H3-15
SPARE Pushbutton H3-8
starting XChecker H3-26
Tiepoints J10 H3-15
Unregulated Power Input H3-7
XC3020A
Download cable connections H3-18
Serial PROM socket H3-19
XC3020A configuration switches H3-16
DOUT (Data Out) H3-17
INP (Input) H3-16
MCLK (Master Clock) H3-17
Mode Pins H3-17
MPE (Multiple Program Enable) H3-16
SPE (Single Program Enable) H3-17
XC3020A FPGA socket H3-16
XC3020A probe points H3-16
XC4003A configuration switches H3-13

FPDA Demonstration Board *(Continued)*
INIT (Initialize) H3-14
Mode Pins H3-13
MPE (Multiple Program Enable) H3-13
PWR (Power) H3-13
RST (Reset) H3-13
SPE (Single Program Enable) H3-13
XC4003A FPGA socket H3-12
XC4003A probe points H3-12
XChecker/Download Cable connections H3-14
frame register U6-22
frames U6-40
framing U6-21
framing error V16-3, V16-44, V16-45
freezing pins F2-24, F2-25, F/ApC-20, F/ApC-22
frequency divider B4-2
From option V15-43
FromAll option V15-43
FromFF V15-29
FromFF option V15-41
FromFF option to XDelay O15-47
FromIOB option V15-43
From–To statement R1-71
FUNC
ADD_SUB B4-15, B4-65
function generators A1-10, L1-101, R2-165, R2-183, R2-184, R2-211
base configuration modes L1-2
carry logic L1-98
carry mode configuration syntax L1-101
grouping with BLKNM attribute L1-5
grouping with HBLKNM attribute L1-16
logic equations for F and G L1-12, L1-102
mapping constraints L1-59
mapping into F L1-59
mapping into H L1-59
merging with MAP attribute L1-30
placement constraints L1-46
specifying with LOC constraint L1-24
function generators *see also* individual carry mode configuration mnemonics
function key, defining action of F2-38
function key R2-255, R2-278, R3-57, R3-64, R3-72, R3-143, V2-14, V2-15, V11-18, V12-26, V16-10
defining in XDelay R3-23
defining in XDM R1-33
functional block A5-9, A7-1, A7-15, A7-16, A7-22
created by OrCAD Draftschematic A1-7
functional simulation A1-1, A1-9, A5-4, A6-6, A6-12, A6-32, A7-23, A9-22, B3-8, M1-2, M6-1, O6-1, R1-116, U2-5, U4-4
auto generate M6-5
back-annotation B3-8
command file V12-35
creating a VST file O10-10
design flow
manual translation V1-4, V10-6, V10-7, V12-2
XSimMake V1-4, V6-3, V12-2
designs with CLB/IOB primitives V6-11, V10-5, V10-6, V10-10
designs with FILE attributes V6-3, V6-8
designs with file attributes V12-29
designs with hard macros V6-8
designs with MemGen components V6-3, V6-11, V12-29
designs with special symbols V1-4, V6-1, V6--3, V6--7, V12-1
designs with X-BLOX modules V6-3, V6-8, V6-10, V10-5, V10-6, V10-9, V12-28, V12-29, V13-11, V13-16

functional simulation *(Continued)*
designs with Xilinx ABEL components V6-3, V6--10, V10-5, V12-28, V12-29, V14-16, V14-20
designs without special symbols V1-4, V6-2, V10-5, V10-8, V12-1, V12-5, V12-29
EPLD M6-2, V1-4, V6-1, V6-7, V10-5, V16-54
designs O6-1, O16-61
EPLD net visibility V9-6
FPGA designs O6-1
creating a VST file O12-10
debugging O12-23
IOB and CLB primitives O6-5, O10-13
manual translation O12-26
summary O12-5
XSimMake program O12-10, O12-25
generating netlist manually V1-4, V6-1, V10-5, V10-11, V16-54
generating netlist with XSimMake V1-4, V6-1, V6-2, V12-1, V12-28, V12-30
input V6-3
LCA2XNF R3-29
manual translation M10-2
output V6-3, V12-31
purpose V6-1
ROMs M9-3
see also PLD_FNCSIM8
simulating in ViewSim V12-35
use original M6-5
viewing waveforms in ViewWave V12-39
X-BLOX designs O10-13, O13-11
Xilinx ABEL designs O14-16
XSimMake program O6-4
FX80 R3-75

## G

G net attribute L1-33, V4-10
G output flag O4-18
gate functions, see Xilinx Libraries Guide for description and selection details
gate models R3-30
gate optimizer F5-9
GBUF component E4-10
GCLK L1-19, L1-27, M11-64, R2-114, R2-124
GCLK primitives U1-9
GCLK symbol V11-89, V/ApE-20
gen_lib M2-2
Gen_Sch8
Error messages M/Ap-4
functional simulation M6-5, M10-5, M10-7, M10-8, M10-11
options M10-24
syntax M10-23
timing simulation M10-17, M10-18
variables M10-23
Gen_Sym8 M3-9
EPLD M5-14
Error messages M/Ap-5
Gen_Sym8 program A5-9
general purpose interconnect U1-11, U9-30
general-message-log report A7-22, A7-23
generic keyword E4-2, E4-3
generic PAL E3-5, E4-2
get command O3-7
getting started
OrCad O2-1
global attributes O5-20, V5-14
global buffers B6-5, L1-46
constraints L1-70
corner designations L1-70
LOC placement examples L1-27
global clock buffers V1-2, V11-88, V11-89, V11-91, V11-112, V11-128
global clock distribution U3-8
global modifications B2-19

global reset signal V9-1, V9-8, V12-17, V/ApD-15
global resources U1-9
ACLK primitives U1-9
BUFGP primitives U1-9
BUFGS primitives U1-9
GCLK primitives U1-9
global set/reset signal B6-6, M9-2, M9-5, V9-2, V9-8, V12-18
globalresetb M9-2, M9-5
GND V3-2, V5-13, V11-141, V11-142, V/ApD-5
GND symbol O4-20
EPLD designs O5-14
GOSC macro
XC3000 Demonstration Board H1-8
go-to-initial-state option A6-9, A6-25
GR signal O10-22
graphic interface R1-18
graphic interface of XDM F2-9
grid V/ApA-24, V/ApC-20, V/ApC-21, V/ApC-22, V/ApC-24, V/ApC-25
Grid menu V/ApC-24
GRID option V/ApD-6
grid-off command V/ApC-24
grid-on command V/ApC-24
gridsize option V/ApD-10
grid-space command V/ApC-25
ground bounce L1-6, L1-39, V4-7
ground signal O10-22
GSR pin V9-2
GSR signal O10-22
GTS signal O10-22
guide file M7-3, R2-165, R2-167, R2-168, R2-170, R2-172, R2-174, R2-175, R2-176, R2-177, R2-178, R2-182, R2-183, R2-185, R2-188, R2-194, R2-195, R2-202, R2-203, R2-207, R2-219, R2-220, V11-139, V11-144
incremental design O11-95
guide option R2-167, R2-168, R2-170, R2-172, R2-177, R2-184, R2-194, R2-202, R2-219, V11-139
guide_blks option R2-178, R2-180, R2-181, R2-182, R2-185, R2-194, R2-202, R2-219
guide_only option R2-178, R2-182, R2-195, R2-203, R2-220
guide_routing option R2-178, R2-180, R2-182, R2-194, R2-203, R2-220
guide_thru_routes option R2-178, R2-180, R2-182, R2-183, R2-195, R2-204, R2-220
guided design
constraints R2-184
definition R2-175
in incremental design R2-175, R2-179
in iterative design R2-175, R2-178, R2-179
in XDE R2-175, R2-180
IOBs R2-176
naming signals R2-176
obtaining best results R2-176
options R2-178
representing internal nodes in XDE R2-176
synthesized logic R2-176
XACT-Performance specifications R2-184
XC3000A/L designs R2-177, R2-184
XC3100A designs R2-177, R2-184
XC4000 designs R2-177
GXTL symbol V9-4, V9-5, V/ApD-2, V/ApF-7

## H

H attribute M5-23
H net attribute L1-33, V5-20
H_SET constraint L1-17, L1-76, L1-77, L1-87, L1-95
hard macros, *see* RPM
hard macros V1-3, V3-5, V6-8
compatibility with unified libraries R1-111, R1-114, R1-118
conversion design flow R1-116

hard macros *(Continued)*
definition R1-111
functional simulation R1-116
HM file R1-112, R1-113, R1-114, R1-116
input pin default values R1-111
LOC constraint R1-113
logic trimming R1-112
processing designs with HM2RPM R1-111
user-created R1-111, R1-112, R1-114
designs with previous library elements R1-113
designs with unified libraries elements R1-113
Xilinx-created R1-111, R1-112, R1-113, R1-114
designs with previous library elements R1-114
designs with unified libraries elements R1-114
hardware description languages R1-2
HBLKNM attribute L1-47, O4-15, V4-4, V15-7
architectures L1-16
purpose L1-16
symbols L1-16
syntax L1-17, L1-46
HBLKNM parameter R2-61, R2-62
header connectors
XC4000 Demonstration Board H2-6
XChecker H5-13
header section (PLUSASM) E2-2
height-limit option V/ApD-11
help A6-39, A6-43
ViewDraw V/ApA-36
ViewWave V/ApC-26
Workview V11-19
XDM V11-15
Xilinx ABLE A2-6, A5-2
help command
accessing through XDM R1-31
Help menu A2-6
PCs A6-16
workstations A6-36
help option A6-46, V/ApD-7
help-about command A6-19
help-adv option V/ApD-11
help-all option A6-39, A6-43, R1-118, R2-35, R2-38, R2-204, R2-217
help-design-process command A6-18
help-devices command A6-19
help-errors command A6-19
help-for-help command A6-18
help-index command A6-18, A6-37
help-keyboard command A6-18
help-language command A6-19
help-menus command A6-19
help-on-ABEL-language command A6-37
help-on-context command A6-37
help-on-devices command A6-38
help-on-error-messages command A6-37
help-on-help command A6-37
help-on-version command A6-38
help-programs-options command A6-19
help-Xilinx-flow command A6-19
hex files F5-16, F/ApC-22, O10-21, V7-1, V7-7, V7-8, V7-10, V10-13, V16-33
creating F2-32
downloading F2-33
XC3000 Demonstration Board H1-14
XPP H4-10
hexadecimal B2-8
hierarchical design *see* design hierarchy L1-16
hierarchical designs E2-2, O3-6, U2-3
sheet path part O3-7
sheet symbol O3-6, O16-56
hierarchical files R2-1
hierarchical names U2-4
high_time parameter R1-87
high-density function blocks (FB) E2-4, L1-33, L1-38, V5-20

using E2-10
high-density-block attribute O5-24
high-impedance
EPLD designs O9-6
high-impedance simulation values A6-14, A6-30
high-impedance Z-value option A6-30
high-level design language (HDL) E1-3
highlight
net O11-85
HM (hard-macro) files R1-111, R1-112, R1-113, R1-116, R1-117
HM2RPM M3-4, O1-4, V1-3, V3-5, V6-8
accessing through XDM R1-21
converting user-created hard macros R1-112
designs with previous library elements R1-113
designs with unified libraries elements R1-113
converting Xilinx-created hard macros R1-113
designs with previous library elements R1-114
designs with unified libraries elements R1-114
creating logic for unconnected input pins R1-112
design flow R1-114
error messages R1-117, R1-119
generating XNF file compatible with previous libraries R1-117, R1-119
generating XNF file compatible with unified libraries R1-117, R1-119
input R1-116, R1-117
invoking
command line R1-117
XDM R1-117
obtaining help R1-118
options
-helpall R1-118
r R1-113, R1-114, R1-117, R1-118, R1-119
outputs
log file R1-117
XNF file R1-113, R1-114, R1-116, R1-117, R1-119
purpose R1-4, R1-111
HM2RPM utility L1-96
hm2rpm.log file R1-117
HMAP V4-3, V4-4, V4-5, V15-10
constraints A1-10, L1-59
mapping constraints L1-59
placement constraints L1-46
relationally placed macros L1-96
schematics example L1-60
unified libraries L1-72
use with BLKNM attribute L1-5
use with HBLKNM attribute L1-16
use with LOC constraint L1-19, L1-20
use with MAP attribute L1-29
use with net attributes L1-34
use with Place Block constraint L1-49
use with RLOC constraint L1-72
HMAP symbols R2-184, R2-191, R2-205, R2-217, U2-4
HMGEN R1-111
hold time V4-7
hold time calculation E5-9
hold violations V9-2, V9-6
home directory R1-12
horizontal longline L1-11, L1-20, L1-69
HP Laserjet R3-76
HU_SET attribute O4-15
HU_SET constraint L1-87, L1-95, V4-6
architectures L1-17
purpose L1-17
purppose L1-82
syntax L1-18, L1-83
HU_SET property M4-8
hyphen V3-1

## I

I input flag O4-18
I net attribute L1-34, V4-10
I/O B2-16
    BIDIR_IO B2-20, B4-2
    block primitives L1-5, L1-16, L1-19
    buffers L1-5, L1-16, L1-25, L1-36
    constraints L1-64
    flip-flops O11-58
    inputs B2-20, B4-1, B4-2
    outputs B2-20, B4-1, B4-2
    pads A1-13, L1-25, L1-46
    pins L1-21, L1-36
    primitives L1-34, L1-72
    registers L1-25
    resource report F3-2
    symbols L1-31, L1-35, L1-40, R2-38, R2-206
IBUF L1-5, L1-8, L1-19, L1-33, L1-39, L1-44, M5-2, V4-7, V5-2, V5-4, V5-7, V5-19, V5-20, V9-2, V12-18, V16-17, V16-18
IBUF component E4-10
IBUF8 V5-14
IDLE U8-10
IE
    BIDIR_IO B4-19
IEEE specification U8-3
IEEE standard 1149.1 U8-1, U8-4, U8-19
IFD L1-5, L1-8, L1-44, V5-2, V5-4, V5-7, V5-11, V5-21, V11-101, V11-102, V15-14
IFDX1 V5-2, V5-7, V5-11
if-then statements A1-13
ignore flag R1-82
ignore parameter R1-101
ignore selected paths R1-81
ignore value V15-10
ignore_maps option R2-184, R2-191, R2-205, R2-217
ignore_rlocs option R2-35, R2-38, R2-184, R2-191, R2-205, R2-217
ignore_timespec option R2-36, R2-39, R2-197, R2-206, R2-219
ignore_xnf_locs option L1-20, R2-35, R2-38, R2-184, R2-191, R2-206, R2-217, V11-116, V11-148
IgnoreCriticalNetFlags U6-2
ignored setting
    dc2p option R2-199
    dc2s option R2-199
    dp2p option R2-196, R2-201
    dp2s option R2-201
    timing option R2-193, R2-215
ILD L1-5, L1-8, L1-44, V5-2, V5-4, V5-7, V5-11, V11-101
implementation M1-2, M7-1, O7-1
    calc design O15-28
    complete design B3-14
    creating files manually O10-15
    LCA file O7-1
    manual translation M10-11
        EPLD M10-13
        FPGA M10-11
    partial design B3-10
    PPR
        log file O15-30
    see also PLD_XEMake
    see also PLD_XMake
    VMH file O7-1
    XEMake O7-1
    XMake O7-1
implementation styles B2-4, B5-1
import
    block O11-42
importing a JEDEC file F2-22
ImproveX A6-40
    error messages A6-6, A6-36, A/ApA-11
    log file A6-6
    optimization A1-10
    purpose A1-6
INC_BY attribute
    INC_DEC B4-65

INC_DEC module B4-64
INC_BY B4-65
RLOC_ORIGIN B4-66
RLOC_RANGE B4-66
STYLE
ALIGNED=Default B4-66
RPM B4-66
USE_RLOC B4-66
INCDEC-F-CI L1-118
INCDEC-FG-1 L1-120
INCDEC-FG-CI L1-118
INCDEC-G-0 L1-119
INCDEC-G-CI L1-120
INCDEC-G-F1 L1-119
INC-F-CI L1-111
INC-FG-1 L1-114
INC-FG-CI L1-111
INC-G-1 L1-112
INC-G-CI L1-113
INC-G-F1 L1-112
INC-G-F3- L1-113
in-circuit verification R1-3, U1-15, U4-9
Design Rule Checker U4-9
download cable U4-9
probe command U4-10
XChecker cable U4-9
include constraint R2-149
include directive A7-3, A7-4, A7-5
include file E1-1, E2-1
include_eqn statement A7-4, A7-18, A7-20, F4-15
incompletely-specified state machines A1-11
incremental design B3-2, M11-4, R2-175, R2-179, V11-139, V11-143
checking changes
XChecker O11-100
configuring XMake O11-98
program settings B3-11
translation O11-99
INET
accessing through XDM R1-21
program O3-8
INF file O10-5
INF2XNF program O10-7
INFF L1-8, L1-19, L1-44
Info menu
ViewDraw V/ApA-36
ViewWave V/ApC-26
info-attr command V/ApA-36
info-help command V2-16, V/ApA-36
info-label command V/ApA-37
info-object-detail command V14-15, V/ApA-37
info-status command V/ApC-26
INIT U8-13
INIT attribute O4-15, V4-4, V9-2, V12-18, V/ApB-24
architectures L1-18
purpose L1-18
syntax L1-18
INIT property M4-5, M9-2, M9-3
initial option A6-48
initial_state option A6-41, A6-44
initialization B2-9
initialization state (INIT) O4-12
INLAT L1-8, L1-44
inpin option V/ApD-11
input
buffers L1-19, O5-2
flip-flops A1-13
levels, XC3000 R2-247
pads E2-4
direct inputs E2-8
registered inputs E2-8
using E2-7
pins, default values R1-111
registers L1-29, L1-38, L1-39
signal polarity F4-67
threshold levels L1-8
vectors
EPLD designs O16-43

input/output blocks *see* IOBs U1-5
input/output properties
see properties.
INPUTPIN (FI)
ABLE-HDL file A7-6, A7-7
statement E2-8, E3-2, E3-18, F4-16
inputs
direct E2-8
hanging F5-7
latched E2-8
registered E2-8
registered with clock enable E2-8
INPUTS module B4-2, B4-68
BOUNDS B4-69
ENCODING B4-69
FLOAT_VAL B4-69
INPUTS B4-68
LOC B4-70
PADNAME B4-69
TNM B4-70
INPUTS pin
BIDIR_IO B4-19
INREG L1-8, L1-44
INST property M4-2
installation procedures for software, see Xilinx Installation Guide for details
installation
partitioning software O2-4
software O2-2
instruction register U8-4
integrate-new-PLD-using-FITEQN command A5-8, A7-18
integration
freezing pins F2-24, F2-25
of a behavioral design F2-24
of a PAL-based design F2-26
of a schematic netlist F2-25
integrator
chip builder module F5-7
design rule checker F5-7
divider module F5-9
interconnector module F5-9
mapper module F5-9
minimizer F5-5
muncher F5-3
netlist reader module F5-3
optimizer module F5-9
partitioner module F5-5
using on example design F/ApC-20
Intel Hex file E1-11, M7-1, M7-7, M10-13
Intel Hex format A1-5
Intel MCS-86 PROM format R2-270, R2-271, R2-274, R2-275, R2-278, R2-279, R2-281
XPP H4-2
interactive mode
XPP Workstation interface H4-23
interconnector integrator module F5-9
interconnects
unused R2-239
interface
command line F2-9
description O1-3
graphic F2-9
libraries O1-3
interior setting R2-38, R2-206
intermediate files A5-10, V11-10
internal IOB R2-147
INTERNAL property M4-8
Intest U8-16
INV attribute V/ApE-10
INVBUS module B4-2, B4-5
INVERT attribute A4-6, A7-14, A/ApB-1
inverters, optimization F5-9
INVMASK attribute B2-9, B4-2, V13-11
IO setting R2-38, R2-206
IOBs L1-67, M6-5, M8-3, M10-3, M10-5, M10-14, U1-5, V/ApF-7
assigning block names to primitives R2-61
attributes V4-8
BASE attribute V4-8
base configuration L1-2

IOBs *(Continued)*
bidirectional R3-18, R3-138
BLKNM attribute V4-3
block definition L1-47
boundary scan U8-9
CMOS attribute V4-8
CONFIG attribute V4-8
configuration tags
XC2000 R3-111
XC3000 R3-111
XC4000 R3-112
configured pins unconnected to nets R3-33
constraints L1-54, L1-67
direct input R3-42, R3-43
direct outputs R3-41
dissociating logical names in XDE R3-190
during boundary scan U8-2
edge designations L1-65
ending points for path delays in XDelay R3-6
external R2-155
FAST attribute V4-7
flagging for internal/external use in XDE R3-140
flattening before mapping in XMake R1-42
flip-flops A1-13, M9-2, R3-41, V11-101, V15-14
half-edge designations L1-66
I pin R3-18, R3-138
I/O constraints L1-64
illegal value on base record R3-36
increasing output speed with FAST attribute L1-13
input clock version R3-42
internal R2-147, R2-155
invalid location in MAP file R2-113
latched input R3-42, R3-43
latches V15-4, V15-6
loadless R2-113, R3-35
LOC constraint V4-5
LOC constraint examples L1-25
location constraints R2-10, R2-47
locking R2-150
logic configuration U7-3
mapping by XMake V11-1
mapping by XNFMAP V7-6, V10-11, V11-144, V11-148
matching to guide file R2-176
merging flip-flops into IOBs B6-4
naming as probes in XDE R3-119
Notplace Instance constraints L1-67
O pin R3-18, R3-138
output 3-state sense inversion R3-42
output clock inversion R3-42
output symbols L1-7
pad signals R2-24
pads L1-7
partitioning in XNFMap R2-168
pin numbers V9-4
placement R2-147, R2-148
placement examples R2-64
primitives R3-36, V6-7, V6-11, V10-5, V10-6, V10-9, V10-10
functional simulation O10-13
prohibit location R2-152
prohibiting logic placement L1-21
Q pin R2-240
registered input R3-42, R3-43
registered outputs R3-41, R3-42
removing default delay L1-35
removing unused in LCA2XNF R3-32
reserved for oscillator V9-4
reserved names V3-2
setting constraint file flag in XDE R3-146
SLOW attribute V4-7
sourceless R2-113
specifying function with CONFIG attribute L1-8

IOBs *(Continued)*
starting points for path delays in XDelay R3-6
symbols L1-13, L1-19, V4-3, V/ApF-7
T pin R3-18, R3-138
three-state buffers A1-13
TTL attribute V4-8
unconfigured R3-34
use with BLKNM attribute L1-5
use with global buffers L1-71
use with LOC constraint L1-72
viewing in XDE V11-127
XC2000 U1-8
XC2000 configuration options L1-9
XC2000L U1-8
XC3000 U1-7
XC3000 configuration options L1-10
XC3000A U1-7
XC3000L U1-7
XC3100 U1-7
XC3100A U1-7
XC4000 U1-5
XC4000 input register R3-42
XC4000 pulldown resistors R3-42
XC4000 pullup resistors R3-42
XC4000A U1-5
XC4000H U1-6
IOPAD L1-7, L1-13, L1-20, V5-3, V5-4, V5-16
IOPIN
ABLE-HDL file A7-6, A7-7
IOPIN (PINFBK) statement E3-15,F4-18
IPAD L1-5, L1-20, M5-2, V5-2, V5-16, V9-2, V11-96, V12-18, V16-18, V16-27
IPAD8 V5-14
Istype keyword A7-13, A7-16, A9-24, A/ApB-2, V14-7
iterative design R2-175, R2-178, R2-179
ivector option A6-48

## J

JED file V7-1, V10-13
JED2HDLX A1-5, A1-6, A7-5, A7-20, A8-1, A8-2
JED2PLD A7-5, A7-21
accessing through XDM R1-21
JED2PLD command F2-22
JED2PLD menu
command E4-4, E4-7
JEDEC A1-5, A1-6, A7-3, A7-4, A7-5, A7-17, A7-18, A7-19, A7-20, A7-21, A8-1, V5-10, V7-1, V7-7, V7-9, V10-13, V16-34
importer F5-15
JEDEC files E1-4, E1-11, F5-15, F5-16
conversion E4-2
creating F2-31
importing into design F2-22

using E4-4
JK flip-flops A1-11, A4-13, A7-14
Johnson counter B4-40
junction V16-22
place O16-21
symbol O11-31, O16-21

## K

K net attribute L1-34, V4-10
K output flag O4-18
Karnaugh maps V14-9
KEEPNAME (KN) attribute B2-23
key macros, *see* macros
KeyCursor command F2-38
accessing through XDM R1-33
keydef command F2-38
accessing through XDM R1-33
example F/ApC-9

## L

L net attribute L1-34, V4-10
L net flag O4-18
label O11-31

components O16-21
wires O16-23
labelpos option V/ApD-15
labels
bus B2-15
last-display-vector option A6-15
last-vector option A6-30
latch enable pins L1-33, L1-34
latch functions, see Xilinx Libraries Guide for description and selection details
latch symbols V/ApD-11, V/ApD-16
latchbflevel option V/ApD-11
latches L1-5, L1-16, L1-19, L1-35, L1-42, M9-2, V4-3, V4-5, V4-7, V4-9, V5-2, V15-4, V15-6
LATCHES set V15-6, V15-7, V15-8, V15-17, V15-19
latchsym option V/ApD-16
LCA U1-1
block names L1-4, L1-49
configuration modes
XC4000 Demonstration Board H2-1
configuration PROMs
XC3000 Demonstration Board H1-13
device part R1-64
reset
XC3000 Demonstration Board H1-13
socket H1-4
LCA file M7-1, M7-4, M7-7, M8-1, M8-3, O7-1, O7-11, U1-13, V1-4, V4-5, V7-1, V7-2, V7-4, V7-6, V7-11, V7-12, V7-13, V8-1, V8-2, V10-5, V10-11, V10-12, V10-14, V10-17, V11-12, V11-119, V11-126, V11-129, V11-139, V11-144, V11-148, V12-1, V12-49, V12-50, V12-54, V13-20, V13-22, V14-23, V14-25, V15-9, V15-23, V15-25
APR R2-131, R2-133, R2-143, R2-144
corrupt R3-33, R3-36, R3-37, R3-39
guide file O11-95
incompletely routed R3-31
incremental design R2-134
input to PPR R2-174
invalid block names R3-36
LCA2XNF R1-5, R3-29
loadless CLBs R3-34, R3-35
loadless IOBs R3-35
loadless pullups R3-35
loadless signals R3-34
loops R3-35
MakeBits R2-228
MAP2LCA R1-4
Map2LCA R2-108
missing part type R3-37, R3-38
output by PPR R2-166, R2-167, R2-168, R2-170, R2-172, R2-174, R2-177, R2-182
sourceless signals R3-34
timing simulation M10-15
XMake R1-3, R1-39
XNFMAP R2-54
LCA2XNF M6-5, M10-5, M10-15, M10-16, U4-4, V10-11, V10-14, V10-17, V10-18, V13-22, V14-25, V/ApD-5, V/ApE-9
accessing through XDM R1-26
creating partitioning guide file in XNFMap R2-55
error messages R3-36
excluding delay information in XNF file R3-32
generating block-only file R3-30
generating delay specification file R3-32
generating EQN symbols R3-30
generating gate-only XNF file R3-31
including delay information in XNF file R3-31
inputs R3-29

LCA2XNF *(Continued)*
options
-b R2-177
outputs R3-29
program description M10-24, O10-16
timing simulation syntax O10-16
purpose R1-5, R3-29
removing unused CLBs and IOBs R3-32
restoring net names (XC4000 only) R3-30
suppressing overwrite warning R3-32
syntax R3-29
-v option R3-32
-w option R3-32
warning messages R3-33
XNF format R3-32
LCB file
output by PPR R2-166, R2-174
LD L1-33, V5-11, V5-21
LD_LIBRARY_PATH M2-2, M11-6, M12-3, M16-2
LDCP L1-5
LE modifier E2-8
LEDs
XC3000 Demonstration Board H1-4, H1-5, H1-6
XC4000 Demonstration Board H2-1, H2-2, H2-5, H2-10
length count U6-1, U6-39, U7-10
alignment U6-44
DONE Alignment method U6-41
Length Count Alignment method U6-44
LEVEL attribute V5-13, V11-82, V11-96, V15-12, V/ApD-12
level-limit option V/ApD-11
Level menu V/ApA-14
Level Pop command V11-77, V11-82, V11-86, V11-89, V11-91, V11-100, V11-102, V11-104, V11-106, V11-110, V11-112, V12-26, V13-9, V14-14, V15-18, V16-52, V/ApA-15
Level Push Schematic command V11-77, V11-78, V11-80, V11-84, V11-88, V11-91, V11-100, V11-102, V11-104, V11-106, V11-108, V11-110, V11-112, V12-24, V12-25, V13-4, V14-12, V14-14, V15-16, V16-52, V/ApA-14
Level Push Sheet command V3-1, V/ApA-15
Level Push Symbol command V11-77, V11-81, V14-15, V/ApA-15
LFSR counter B4-40
cascading counters B4-45
LIB file O3-10
LibEdit O3-8, O4-21
libraries
adding to search path
symbol O3-10
constraints O4-2
creating a netlist file O3-8
creating a symbol O3-8
creating libraries O3-7
creating schematics O3-8
description O1-3
old vs. new libraries O4-2
saving a symbol O3-9
user-created libraries O3-7
X-BLOX library O13-10
library
directory contents F5-13
loading B3-5
library aliases V2-5, V2-8, V2-11, V2-12, V3-5, V3-8, V11-8, V11-13, V11-45, V/ApD-2, V/ApF-1, V/ApF-5
library alias-maintenance facility *see* Altran
library components E4-1
library elements
architectural resources U2-2
macros U2-1
primitives U2-1

library PLD V16-15
library symbols O3-7
copy O11-38
definition O3-7
move O11-39
Xilinx symbols O11-45
LIBVER attribute V11-82, V11-96, V13-9, V15-12
LIFO B4-92
limit setting R2-211
LINK keyword O3-4
LINK parameter R1-100
linked equations E5-3
linking multiple sheets O3-5
list boxes A2-5
list option A6-45
listing option A6-39
listing-file option A6-27
listref M2-8
little–endian B2-18
LL file U7-13
MakeBits R2-228
LOAD
ACCUM B4-9
COUNTER B4-37
reload schematic O11-49
SHIFT B4-94
loading
alternative configurations U6-25
external source for CCLK U6-24
lead device method U6-24
loadless signals R2-42
loadlevel option V/ApD-12
loadm command V6-11, V/ApB-23, V/ApB-24
LOC (EPLD) property M5-18
LOC attribute O4-15
ANDBUS B4-3
BIDIR_IO B4-20
DATA_REG B4-51
INPUTS B4-70
OUTPUTS B4-82
SHIFT B4-98
TRISTATE B4-111
LOC constraint L1-55, L1-57, R1-113, R2-184, R2-191, R2-206, R2-217, V4-5, V5-16, V11-96, V11-115, V15-10, V16-27, V/ApE-3
architectures L1-19
area constraints L1-23, L1-99
BUFT placement examples L1-26
carry logic L1-99
CLB placement examples L1-24
decode logic placement examples L1-28
global buffer placement examples L1-27
global buffers L1-70
ignoring in XNFPrep R2-38
IOB placement examples L1-25
multiple constraints L1-24
prohibit constraints L1-23, L1-99
propagation through flattening L1-94
purpose for EPLDs L1-20
purpose for FPGAs L1-19
single constraints L1-22, L1-99
syntax L1-46
syntax for EPLDs L1-22
syntax for FPGAs L1-21
LOC parameters R2-61, R2-62, R2-121
LOC property M4-6
adding to symbols M4-6
LOC options
XC2000, XC3000 Edit menu O4-10
local-feedback equation (FBK) F4-54
local-shift equation (SHIFT) F4-61
location R2-146
attributes B2-27
constraint R1-113
maps M2-2
properties
see properties.

location *(Continued)*
statements
XC2000 and XC3000 designs O4-10
lock-block constraint R2-150
lock-IOBs constraint R2-150
lock-net constraint R2-151
lock-pin constraint R2-151
lock_routing option R2-178, R2-180, R2-182, R2-183, R2-195, R2-207, R2-220
locked block R2-147
LOG file
log file F5-1, F5-16, V/ApA-19, V/ApB-11, V/ApB-21
MemGen R1-60
output by PPR R2-174
LOG/iC (PLD compiler) E1-3
logfile option R2-33, R2-39, R2-189, R2-207, R2-217
logic
collapser E5-22, E5-25
levels A1-10, A1-11, A4-4, A9-13
minimization V5-18
moving into FFB E5-26
optimization L1-36, V5-17, V5-18, V16-36
optimizer report F3-16
reduction U5-2
resource report F3-2
Logic Cell Array M7-1
Logic Cell Array *see* LCA
LOGIC_OPT attribute O5-21, V5-17, V5-18
architectures L1-28
purpose L1-28
syntax L1-28
LOGIC_OPT property M5-16, M5-20
LOGIC_OPT statement E5-25
logical partition statements E5-3
LOGICAL style B4-97
logic-optimization and device-assignment report A7-22
logic-optimizer report V16-36
longline net attribute *see* L net attribute
longlines R2-127, U1-10, U9-31, V4-10
lower-level files R2-1
LOWPWR attribute V5-16, V5-17
architectures L1-29
purpose L1-29
syntax L1-29
LOWPWR property M5-19
LOWPWR=ALL attribute M5-16, O5-21
LS_IN
SHIFT B4-95
LS_OUT
SHIFT B4-96
LSB L1-103, L1-104, L1-106, L1-107, L1-109, L1-110, L1-112, L1-113, L1-115, L1-116, L1-117, L1-119
LST file A1-8, A5-7, A6-5, A6-27, A6-35

## M

M0/RTRIG U7-8
M0RT V3-2
M1 pin pullup (XC4000 only) R2-248
M1/RDATA U7-8
MAC file R1-60
macro files A1-7, A5-9
macro3.mac O2-12
macros list O2-14
Vstmac.mac O2-12
macros list O2-15
macro option A6-49
macro symbols L1-93, V5-15
macrocell feedback A7-10, A7-12
macro-cell option A6-29
macro-cell-format option A6-14
macrocells A6-14, A6-49, L1-29, L1-33, L1-36, L1-39, L1-44
macros U2-1
creating for multiple instances in XDE R3-116
EPLD M5-13
user-defined M5-14

macros *(Continued)*
FPGA M3-4
Hard M3-4
HM2RPM M3-4
RPM M3-4
Soft M3-4
hard macros O4-2
key macros O11-15
MAK file R1-50
RPMs O4-2, O11-45, O11-47
soft macros O4-2
Viewing O11-45
supplied by Xilinx O4-2
main menu F/ApC-6, F/ApC-7
main screen in XDM R1-10, R1-16
MAK file M7-3, M7-6, M7-8, R1-38, V7-2, V7-4, V7-7, V7-9, V7-10, V7-11, V7-12, V7-13, V7-14, V13-19, V14-22
example R1-46, R1-49
macros R1-50
purpose R1-46
recursion R1-56
syntax R1-46
XMake R1-38
MakeBits M7-4, R2-270, R3-65, U3-3, U3-7, U4-9, U6-1, U6-2, U6-5, V7-1, V7-6, V11-10, V11-12, V14-23
accessing through XDM R1-26
adding delay to LCA file R3-31
assigning configuration tags R3-114
checking circuitry on download cable R2-268
commands
changing startup and configuration options R2-246
checking circuitry on download cable R2-268
creating ASCII bitstream file R2-265
defining function keys R2-255
defining mouse button functions R2-260
displaying net information R2-263
displaying profile settings R2-268
downloading bitstream to LCA device R2-253
executing XDE command file R2-255
exiting MakeBits R2-255
generating bitstream R2-256
invoking DRC R2-253
reading specified bitstream file R2-265
restoring tied interconnects to unused state R2-266
options
creating file of flip-flop output locations R2-259
displaying messages during tiedown R2-258
reflecting effects of tiedown on timing R2-258
tying unused interconnects R2-256
using critical nets last in tiedown R2-259
saving information to text file R2-266
saving options to makebits.pro file R2-267
selecting startup sequence R2-251
setting LCA device startup options R2-246
setting options to makebits.pro file R2-266
setting printer type R2-263
specifying download cable port R2-261
suspending MakeBits R2-253
writing bitstream buffer to file R2-269
writing bitstream mask file R2-260

MakeBits *(Continued)*
configure command
options
aborting readback sequence R2-249
activating LCA Done signal R2-250
adding pullup/pulldown to M1 pin R2-248
adding pullup/pulldown to TDO pin R2-248
enabling CRC R2-248
enabling crystal oscillator amplifier R2-247
enabling pullup resistor on D/P pin R2-246, R2-247
enabling pullup resistor on Done pin R2-248
including flip-flop and latch contents in bitstream R2-249
reading back configured LCA device R2-246, R2-247
releasing I/O from three-state condition R2-250
releasing set-reset to latches and flip-flops R2-251
selecting clock to synchronize release of Done pin R2-249
setting configuration clock rate R2-248
setting Done timing R2-247
setting global reset timing R2-247
setting LCA input threshold level R2-246, R2-247
setting readback clock R2-249
synchronizing I/O startup sequence to Done In signal R2-249
creating a configuration set R2-259
creating ASCII bitstream file R2-265
defaults command
options
ensuring compatibility between XC4000 and XC3000 devices R2-251
ensuring XC4000 compatibility with XC2000, XC3000 R2-252
ensuring XC4000 incompatibility with XC2000, XC3000 R2-252
synchronizing GSR and I/O release to Done In signal R2-252
defining function keys R2-255
defining mouse button functions R2-260
displaying net information R2-263
displaying profile settings R2-268
downloading bitstream to LCA device R2-253
DRC command
options
checking only specified block R2-254
checking only specified net R2-254
checking unrouted design R2-254
displaying information on DRC R2-254
issuing progress status R2-254
skipping block checking R2-254
skipping net checking R2-254
examples R2-243
executing XDE command file R2-255
exiting R2-255
FPGA Demonstration Board H3-25, H3-27
generating bitstream R2-256
inputs R2-228
interaction with XDE R2-244
invoking DRC R2-253

MakeBits *(Continued)*
makeconfigset command R2-259
-mbo= option R2-243
options R2-229, U6-38
creating logic allocation file R2-237
creating rawbits file R2-229
disabling pullup resistor for Done pin R2-238
displaying help screen R2-237
displaying status messages R2-242
generating mask file R2-237
renaming configuration bitsream file R2-238
running Design Rules Checker R2-230
saving tied design R2-238
setting CMOS input signal thresholds R2-229
setting XC4000 configuration R2-230
specifying crystal oscillator options R2-239
specifying D/P pin timing R2-242
specifying readback options R2-239
specifying reset timing R2-243
tying unused interconnects R2-239
outputs R2-228
purpose R1-5, R2-227
reading specified bitstream file R2-265
restoring tied interconnects to unused state R2-266
saving information to text file R2-266
saving options to makebits.pro file R2-267
screen R2-244
selecting startup sequence R2-251
setconfigset command R2-268
setting LCA device startup options R2-246
setting options to makebits.pro file R2-266
setting printer type R2-263
specifying download cable port R2-261
suspending R2-253
syntax R2-227
Tie U6-2
tie changes to net delays R2-264
writing bitstream buffer to file R2-269
writing bitstream mask file R2-260
XC2000 configuration
enabling pullup resistor on D/P pin R2-246
reading back LCA device R2-246
setting LCA input threshold level R2-246
XC3000 configuration
enabling crystal oscillator amplifier R2-247
enabling pullup resistor on D/P pin R2-247
reading back configured LCA device R2-247
setting Done timing R2-247
setting global reset timing R2-247
setting LCA input threshold level R2-247
XC4000 configuration
aborting readback sequence R2-249
activating LCA Done signal R2-250
adding pullup/pulldown to M1 pin R2-248
adding pullup/pulldown to TDO pin R2-248
enabling CRC R2-248
enabling pullup resistor on Done pin R2-248
including flip-flop and latch contents in bitstream R2-249
releasing I/O from three-state condition R2-250

MakeBits, XC4000 configuration *(Continued)*
releasing set-reset to latches and flip-flops R2-251
selecting clock to synchronize release of Done pin R2-249
setting configuration clock rate R2-248
setting readback clock R2-249
synchronizing I/O startup sequence to Done In signal R2-249
XC4000 Demonstration Board H2-13, H2-15
XDE version R2-227
XMake version R2-227
running in XMake R1-41
XPP H4-2
makebits.pro file R2-266
makeconfigset command
MakeBits R2-259
MAKEJED V7-1, V7-7, V10-13
accessing through XDM R1-26
command F2-31
menu
command E3-9
example E1-11
MakeLL U6-2
MAKEPRG V7-7, V7-10, V10-13
accessing through XDM R1-26
command F2-32
example F/ApC-22
menu
command E3-9
example E1-11
MAKEPROM R3-65, U6-1, U6-3, U6-5, U6-6, V7-1
accessing from XDE R2-270, R2-273
accessing through XDM R1-27
changing mouse button functions R2-279
clearing PROM memory files fom RAM R2-275
commands
clearing memory files from RAM R2-275
defining function keys R2-278
defining mouse button functions R2-279
displaying current MakePROM settings R2-282
displaying current PROM size R2-280
executing command file R2-276
executing commands in makeprom.pro file R2-281
exiting MakePROM R2-277
loading bitstream file R2-278
printing MakePROM screen R2-280
removing file from PRM memory in RAM R2-275
saving data into file R2-281
saving MakePROM settings in makeprom.pro file R2-281
selecting PROM format R2-278
setting PROM size R2-282
suspending MakePROM R2-276
defining function keys R2-278
displaying PROM size R2-280
displaying value settings R2-282
examples R2-273
executing command file R2-276
executing makeprom.pro file R2-281
exiting and returning to XDE R2-277
FPGA Demonstration Board H3-25, H3-27
loading BIT file at specified address R2-278
menus
Misc R2-274
Profile R2-274
Prom R2-274

MAKEPROM *(Continued)*
options
displaying help screen R2-271
displaying messages R2-273
loading BIT files down from hex address R2-271
loading BIT files up from hex address R2-272
loading BIT files up or down from next address R2-271
setting PROM format R2-271
setting PROM size R2-272
specifying PROM output file name R2-272
outputs R2-270
printing screen R2-280
purpose R1-5, R2-270
removing files from PROM memory in RAM R2-275
saving information to file R2-281
saving settings in makeprom.pro file R2-281
screen
command prompt R2-273
PROM memory table R2-274
status bar R2-274
selecting PROM format R2-278
specifying PROM size R2-282
stand-alone version R2-270
suspending and returning to DOS R2-276
syntax R2-270
XC3000 Demonstration Board H1-9
XC4000 Demonstration Board H2-13, H2-15
XChecker H5-8
XPP H4-2
makeprom.pro file R2-281
makesym option V/ApD-7
manipulating XACT-Performance parameters in XNFMerge R2-13
manual translation M10-1, O10-2
program summary M10-18
manual-pin assignment E5-2
MAP attribute L1-62, O4-15, V4-4, V/ApE-1
architectures L1-29
purpose L1-29
syntax L1-30
MAP file R2-43, R2-44, R2-69, R2-71, V7-6
input to PPR R2-165, R2-174
MAP2LCA R1-4
Map2LCA R2-107, R2-108, R2-113
output by XNFMap R2-168, R2-172, R2-174
signal binding R2-6
symbols R2-6
XNFMerge R1-4, R2-1, R2-2, R2-6
MAP mapping report file F/ApC-21
MAP2LCA M10-15, M10-17, U3-2, U5-2, V7-6, V10-11, V11-12, V/ApD-2
accessing through XDM R1-21
design.map file R2-107
error messages R2-115
example R2-109
inputs
MAP file R2-107
options
ignoring MAP file placement constraints R2-108
specifying LCA device R2-108
outputs
AKA file R2-108
LCA file R2-108
SCP file R2-108
purpose R1-4, R2-107
syntax R2-107
warning messages R2-113
map-file=-then-merge M7-4
mapped_xnf option A6-43
mapper integrator module F5-9

mapping U1-15, U2-4, U3-5
  place in design implementation R1-2
mapping control symbols L1-5
mapping report A7-22, F3-4, F/ApC-21, V16-36
mapping your design R2-43
map-then-merge M7-4
margin delays R3-17, R3-27
  clearing in XDE R3-103
  reading from MRG file in XDE R3-169
  saving in XDE R3-175
mask file R2-229, U7-4
master parallel mode U6-8, U6-16
master serial mode U6-11, U6-18
max. clock freq. calculation E5-10
maxclbs option A6-39
maximal encoding A3-6
maxpaths option V15-40
maxsheet option V/ApD-16
MBA file M10-15
MBAPP M10-15
MCS–86 format R2-270, R2-271, R2-274, R2-275, R2-278, R2-279, R2-281
  XPP H4-2
MEDFAST attribute O4-16, V4-7, V11-100
  architectures L1-31
  purpose L1-31
  syntax L1-31
MEDFAST property M4-9
MEDSLOW attribute O4-16, V4-7, V11-100
  architectures L1-31
  purpose L1-31
  syntax L1-31
MEDSLOW property M4-9
megafile format V2-5, V3-8, V11-8, V/ApE-15
MEM file R1-59, R1-60, V6-11
  comments R1-63
  data command R1-62
  default command R1-62
  depth command R1-61
  MemGen R1-59
  memory characteristics R1-61
  symbol command R1-61
  type command R1-61
  width command R1-61
MEMFILE attribute
  PROM B4-85
  Syntax B4-86
MemGen L1-57, L1-58, M3-9, M6-3, M8-3, M10-3, M10-14, R2-170, U2-2, V4-14, V7-5, V12-29
  accessing through XDM R1-21
  checking address boundaries R1-66
  data formats R1-63
    base R1-63
    value R1-63
  example R1-66
  functional simulation V1-3, V6-7, V6-11
  inputs
    MEM file R1-59, R1-60
  merging files with XNFMerge V7-6, V10-4
  options
    creating OrCAD/SDT symbol R1-64
    creating Viewlogic Viewdraw symbol R1-65
    old_library= R1-65
    specifying bus notation R1-64
    specifying LCA device R1-64
    specifying memory depth R1-64
    specifying memory type R1-64
    specifying memory word width R1-64
  options and parameters R1-64
  outputs
    log file R1-60, R1-65
    macro files R1-60
    OrCAD/SDT LibEdit command files R1-60
    XNF files R1-60

MemGen *(Continued)*
purpose R1-3, R1-59
ROMs V1-4
simulation schematics V12-33
symbols V1-3
syntax R1-59
timing simulation V1-3, V12-49
MemGen design files
merging into OrCAD design files O4-21
MemGen program O4-21
memmiser option A6-39
memory
depth R1-61
PROM B4-2, B4-84
SRAM B4-2, B4-106
symbol R1-61
type R1-61
width R1-61
memory definition file R1-59
PROM B4-85
memory elements, see Xilinx Libraries Guide for description and selection details
men2xnf8 M6-1
.log M6-7, M7-8
log file M7-8
manual translation M10-1
options M10-25
.sh M6-7
see also PLD_Men2XNF8
syntax M10-24
variables M10-24
Mentor A5-9, L1-2, L1-43
menu bar R1-10, R1-16
menu colors
command F2-39
accessing through XDM R1-33
defining in XDM R1-33
menus
Design Entry F2-18
Fitter F2-24
main F2-3, F/ApC-6, F/ApC-7
opening F2-9, F2-17
Profile F2-38
structure O11-14
Translate F2-18
Utilities F2-33
Verify F2-28
XDM F2-16
mergeio option B/Ap-2, V10-9
merge-then-map M7-4
merging U3-5
third-party designs O4-20
XNF files F2-23
messages F5-16
directory F5-13
MGC_GENLIB M2-2, M11-6, M12-3, M16-2
MGC_HOME M2-1, M11-6, M12-3, M16-2
MGC_LOCATION_MAP M2-2, M11-6, M12-3, M16-2
MGC_WD M2-2, M12-4, M16-3
MINC U2-3
minimization A6-8, A6-11, A6-27, A6-47, A7-14
MINIMIZE attribute O5-21, V5-18
architectures L1-31
purpose L1-31
syntax L1-32
MINIMIZE property M5-16, M5-20
MINIMIZE statement F4-23
minimizer integrator module F5-5
turning off for an equation F5-7
minsheet option V/ApD-16
Misc menu R2-274
misc-report command V15-32, V15-33, V15-40, V15-42
mode buttons A2-4
mode pins
XC4000 Demonstration Board H2-12

mode switches
FPGA Demonstration Board H3-26, H3-27
XC4000 Demonstration Board H2-14, H2-15
mode/connection port F2-18
model for simulation, creating F/ApC-23
models
QuickSim II simulation M9-1
modes
asynchronous peripheral U6-19
master U6-7
Master Parallel Up/Down U6-8
master parallel Up/Down U6-16
Master Serial U6-11
master serial U6-18
non-master U6-7
Peripheral Mode U6-13
Slave Mode U6-14
slave serial U6-20
synchronous peripheral U6-18
XC2000 U6-7
XC3000 U6-7
XC4000 U6-16
modgen option B/Ap-2
Modify menu V/ApC-15
modify property M3-8
modify-bus command V/ApC-16
modify-expand command V/ApC-16
modify-invert command V/ApC-15
module
*see also* X-BLOX modules, attributes
data values B2-6
module block type V3-9, V5-12, V14-14, V14-15, V14-20, V/ApA-18
module names A4-17
module ports O11-33
module statement A3-10, A3-15, A6-12, A9-19, A9-23, V14-6
module-arguments option A6-12
Motif F2-4
Motorola EXORMAX PROM format H4-2, R2-270, R2-271, R2-274, R2-278, R2-281
mouse
changing configuration in XDE R3-147
configuration R3-66
configuration in XDM F2-5, O16-12, R1-12, R1-18
defining buttons in XDelay R3-23
defining buttons in XDM R1-33
mouse button V2-14, V11-17, V16-9, V16-11
configuration in XDM F2-9, F/ApC-8
functions, changing F2-39
settings F2-9, F/ApC-8
mouse command F2-39
accessing through XDM R1-33
options
done R2-261
menu R2-261
select R2-261
switch R2-261
mouse settings field F2-18
move
library symbols O11-39
move command V11-50, V11-94, V15-11, V16-17, V16-21, V16-26, V/ApA-29, V/ApA-33
Move menu V/ApA-33
MR pin V9-6
MRG file
XNFMerge R2-3
MRINPUT attribute O5-21, V5-18
architectures L1-32
purpose L1-32
syntax L1-32
MRINPUT property M5-16, M5-23
MS_IN
SHIFT B4-95
MS_OUT
SHIFT B4-96
MSB L1-102, L1-105, L1-108
MSG directory F5-13

multiple program enable
XC4000 Demonstration Board H2-11
multiple source files A7-3, A7-4
multiple state machines A9-14
multiple-sheet designs O3-3, V3-1
I LINK keyword O3-4
flat designs O3-3
hierarchical designs O3-6
multiple-source files A7-17
multiplexer functions, see Xilinx Libraries Guide for description and selection details
multiplexers
MUXBUS B4-72
MUXBUS2 B4-74
MUXBUS4 B4-76
MUXBUS8 B4-78
muncher integrator module F3-2, F5-3
MUX_IN
MUXBUS B4-72
MUX_OUT
MUXBUS B4-73
MUXBUS2 B4-75
MUXBUS4 B4-77
MUXBUS8 B4-79
MUXBUS
Select warning message B4-72
MUXBUS module B4-2, B4-72
MUXBUS2 module B4-2, B4-74
Select warning message B4-74
MUXBUS4 module B4-2, B4-76
Select warning message B4-76
MUXBUS8 module B4-2, B4-78
Select warning message B4-78
MUXBUSx V13-10
mwmrc file F2-4, R1-12
my-text-editor-is command A5-3, A6-5

## N

N net attribute L1-34, V4-10
name buses O11-34
name reference file, *see* NRF file
naming conventions M3-1, V3-1
symbols and nets O3-1, O4-2
nets and subnets O3-2
reserved names O3-1
valid characters O3-2
NAND gates
optimization F5-9
NAND gates, see Xilinx Libraries Guide for description and selection details
narrow_menus attribute V11-17
navigating through directories F2-34
neg attribute A4-6, A6-11, A6-27, A7-14, A7-16
negative equations A7-15
net attributes
architectures L1-32
C L1-33, V4-10
entering V3-7, V11-97
EPLD V5-15
F L1-33, V5-20
G L1-33, V4-10
H L1-33, V5-20
I L1-34, V4-10
K L1-34, V4-10
L L1-34, V4-10
N L1-34, V4-10
P L1-34, V4-10
purpose L1-33
S L1-34, V4-10
supported devices V4-11
syntax L1-35
W L1-34, V3-7, V4-10
X L1-35, V4-10
net locations R2-213, R2-219
net naming conventions V3-1, V3-2
NET properties M4-13
see also properties.
net weight R2-146
NETFLAG (EPLD) property M5-22
NETFLAG property M4-13

net-hightlight command V11-129
netlist
  file F5-3, F5-15, O3-8
  integrating F2-25
  merging multiple files F2-23
  OrCAD, creating F2-21
  reader integrator module F5-3
  reading F5-3
  Workview, creating F2-21
net–locked block R2-147
NETNAME option V10-24, V/ApD-6
netnet option V/ApD-12
nets R2-146
  adding in XDE R3-95
  adding pins in XDE R3-96
  altering routing in XDE R3-127
  analyzing M9-1
  assigning to pins in XDE R3-97
  assigning to predefined probe in XDE R3-97
  assigning weight in XDE R3-193
  clock R3-14, R3-15, R3-17, R3-27
  coloring in XDE R3-105
  coloring interconnects in XDE R3-141
  configuring interconnects in XDE R3-172
  deconfiguring in XDE R3-191
  delays R3-29
  deleting in XDE R3-122
  deleting pins in XDE R3-120
  displaying information in XDE R3-163
  displaying scrolling menus in XDE R3-152
  dissociating from probes in XDE R3-190
  ending points for path delay in XDelay R3-6
  flagging with attributes in XDE R3-140
  highlighting a net O11-85
  highlighting in XDE R3-185, R3-192
  ignoring paths in XDelay R3-8
  merging in XDE R3-143
  moving connections between blocks in XDE R3-148
  moving window to in XDE R3-137
  multiple connections to pin R3-36
  removing connections from world view in XDE R3-192
  remove highlighting in XDE R3-191
  renaming in XDE R3-152
  reporting information in XDelay R3-20
  restricting path tracing with -Netfilter option R3-8
  saving information to text file in XDE R3-171
  setting constraint file flag in XDE R3-146
  split logical R3-30
  splitting in XDE R3-186
  starting points for path delay in XDelay R3-6
  swapping connections on blocks in XDE R3-186
  unrouted in LCA file R3-33
never setting R2-211
no_look attribute V11-17
node (UIM) statement E2-13
NODELAY attribute O4-16, V4-7
  architectures L1-35
  purpose L1-35
  syntax L1-36
NODELAY property M4-8
nodes
  assigning to outputs E3-15
  assignment (in PALCONVT) E3-2
  declarations A4-16
  splitting E5-12
  statement E3-2, F4-25
nodetrst property A7-10
no-listing option A6-12
non-critical flag O4-19
non-critical net attribute *see* N net attribute

none setting R2-38
guide_thru_routes option R2-183, R2-204
ignore_locs setting R2-206
ignore_timespec option R2-206
lock_routing option R2-183, R2-207
non-primitive symbols R2-5, R2-10, R2-11, R2-14
no-optimize option A6-40
no-reduction option A6-11, A6-27, A7-15, A7-16
NOR gate functions, see Xilinx Libraries Guide for description and selection details
norestore U6-2
noschem option V/ApD-7
NOT(inversion)
optimization F5-9
Notplace Block constraints L1-49
Notplace Instance constraints L1-48, L1-54, L1-63, L1-67
no-trace option A6-13
NRF file O10-20, O10-21
*see also* recycled aliases

## O

O option A6-45, A6-47, A6-48
obsolete libraries M3-4
OBUF L1-5, L1-7, L1-8, L1-13, L1-15, L1-19, L1-44, M5-2, V5-2, V5-3, V5-4, V5-5, V5-11, V5-18, V5-21, V9-7
OBUF components R2-126
OBOF functions, see Xilinx Libraries Guide for description and selection details
OBUF8 V5-16
OBUFE L1-15, V5-2, V5-3, V5-18
OBUFEX1 V5-2, V5-3
OBUFEX1 component E4-12, E4-13
OBUFT L1-5, L1-7, L1-8, L1-13, L1-44, V5-2, V5-3, V5-11
OBUFT components R1-107, R1-108
OBUFZ components R1-107, R1-108
octadecimal B2-6
octal B2-8
OE
BIDIR_IO B4-19
TRISTATE B4-110
OFD L1-5, L1-8, L1-13, L1-44, V11-101
OFDI L1-13
OFDT L1-5, L1-8, L1-13, L1-44, V5-11, V11-101
OFDTI L1-13
ok button A2-4
ok setting R2-211
old_library option A6-40
old_library option A6-43
one_hot encoding B2-17
ONE_HOT style
COUNTER B4-40
DECODE B4-59
one-hot encoding A6-9, A6-25, A6-35, A6-38, A6-42, U3-4
definition A3-6
EPLDs A3-6
example A9-1, A9-5, A9-14
FPGAs A3-6
limitations A3-7
OPAD L1-5, L1-7, L1-13, L1-20, M5-2, V5-2, V5-5, V5-16, V16-27
opcodes V11-108, V11-109, V11-136, V11-137, V12-17, V12-19
open ABEL I format A6-45, A6-47
open ABEL II format A6-47
Open-ABEL file A1-8
Open-ABEL2 file A1-8
Open-ABLE file A1-6
Open-ABLE2 file A1-6, A5-4, A6-11, A6-16, A6-31, A6-33, A6-45, A6-46
opening a menu F2-9, F2-17
openlook R1-12
open-sheet command M3-7
openwindows F2-4

operating modes B2-6
OPT attribute V5-17, V9-7
architectures L1-36
purpose L1-36
syntax L1-36
OPT property M5-19
optimization B6-4, E5-22, U1-15, U3-4
area vs. speed A1-9, A1-13, A6-38, A6-39, A6-41, A9-5
binary encoding U3-4
compromises A3-5
DATA_REG module B4-52
don't-care A4-17
EPLDs A5-6, A6-11, A6-26, A7-22
example A9-5
FPGAs A5-5
logic levels A1-10, A9-13
minimization A6-8, A6-11, A6-24, A6-27, A6-47, A7-14
one-hot encoding U3-4
options A5-5, A5-6, A6-9, A6-25, A6-43, A7-16
place in design implementation R1-2
satate machine speed A6-41
standard encoding U3-5
state machine speed A6-44
state-machine speed A1-11, A6-10, A6-26
XOR gates A7-16
optimization effects E5-4
optimization options A6-25
optimize option A6-9, A6-43
optimizer E5-5
optimizer integrator module F3-2, F5-9
optimizing device resources E5-22
option boxes A2-5
option syntax, *see* X-BLOX options
options command F2-39
accessing through XDM R1-33
auto-make A1-12
auto-update A1-12
Options menu
PCs A6-15
workstations A6-23
options-auto-make command A5-4, A6-31
options-auto-update command A5-4, A6-15, A6-18
options-compile command A5-4, A6-27
options-compile-listing-file command A5-7
options-editor command A5-3, A6-32
options-program-pause command A6-16, A9-26
options-read-only command A6-16
options-simulate command A5-4, A6-28
options-spaces-to-tabs command A6-16
options-Xilinx-EPLD command A6-26
options-Xilinx-EPLD-netlist command A5-6
options-Xilinx-FPGA-netlist command A1-9, A1-10, A1-11, A5-5, A6-23
OR gate functions, see Xilinx Libraries Guide for description and selection details
OR gates R2-5
ORBUS module B4-2
ORBUS1 module B4-2, B4-6
ORBUS2 module B4-2, B4-6
ORBUS2 symbol V13-10
OrCAD A1-5, A7-18, A7-19, A7-20, A7-23
file format conversion F2-29
input to XMake R1-38
netlist, creating F2-21
VST simulation file F2-29
OrCAD (VST)
accessing through XDM R1-27
OrCAD draft A1-7, A5-9
OrCAD VST E5-4
OrCAD/ESP, *see also* ESP
configuration O2-6
invoking
from DOS O2-5
from XDM O2-5

OrCAD/SDT
register ordering R2-51
OrCAD/SDT LibEdit command file R1-60
OrCAD/SDT symbol R1-64
OrCADPLD (PLD compiler) E1-3
OSC symbol V9-4, V9-5, V/ApD-2, V/ApE-4, V/ApF-7
OSC4 symbol V/ApF-7
OSC4_IN signal O10-23
oscillators V3-2, V3-4, V9-4, V11-11, V11-88, V11-90, V15-24, V15-29, V/ApF-7
XC3000 designs O11-49
XC4000 designs O11-51
otherxnf subdirectory V8-3, V14-19
out file M7-8, V7-11, V11-119, V11-120, V11-121, V11-145, V12-31, V15-24
APR R2-135, R2-156
outbflevel option V/ApD-12
OUTFF L1-8, L1-19, L1-44
OUTFFT L1-8, L1-44
OUTFFT components R1-107, R1-108
OUTFFZ components R1-107, R1-108
outfile option R2-36, R2-40, R2-175, R2-189, R2-208, R2-217
out-of-range indicators B2-13
outpin option V/ApD-12
output
buffers L1-19, O5-2, O5-4
drive levels L1-8
enab./disable time calc. E5-10
enable signals E3-17
files
warning messages O11-76
flip-flops A1-13
pad structures E2-4
using E2-17
polarity F4-66
spc file
LCA2XNF -s option R3-30
output functions, see Xilinx Libraries Guide for description and selection details
output_directory option A6-40, A6-43
output_xnf option A6-40, A6-43
outputpin
ABLE-HDL file A7-6, A7-7
statement E2-18, E3-2, E3-15, F4-30
outputs
direct E2-18
splitting E5-18
tri-state E2-17
OUTPUTS module B4-2, B4-80
BOUNDS B4-81
ENCODING B4-81
FLOAT_VAL B4-81
LOC B4-82
PADNAME B4-81
TNM B4-82
output pin
BIDIR_IO B4-19
ovector option A6-45
overlap attribute V11-17
overlapping objects
cleaning up F2-20
overrun error V16-3
overview F1-1, F5-1
behavioral design entry F1-9, F1-10
schematic capture F1-7
XDM F1-2
OVFL
ACCUM B4-11
ADD_SUB B4-15, B4-65

## P

P net attribute L1-34, V4-10, V/ApE-2
P option A6-42
p2p R1-86, R1-90
p2s R1-86, R1-88
overlapping specifications R1-88
package pins V3-2
pad L1-5, L1-20
pad bits U6-5

pad names L1-51
pad primitives L1-5, L1-16
pad registers L1-39
pad symbols L1-19, L1-20, L1-21, L1-64, L1-66, V4-7, V5-3, V5-16
PADNAME attribute
  BIDIR_IO B4-20
  INPUTS B4-69
  OUTPUTS B4-81
pads L1-42
pads set V15-6, V15-7, V15-8, V15-14, V15-17, V15-19
pad-to-clock path delay V15-9
PadToPad option V15-29, V15-39
pad-to-pad path delay V15-33
pad-to-pad paths R2-196, R2-200, R2-219
PadToSetup option V15-29, V15-39
pad-to-setup path delay V15-9, V15-12, V15-33
pad-to-setup paths R2-201, R2-219
PADU L1-5
PAL A7-4, V6-8
  20V8 E1-4, E3-2, E3-4
  22V10 E1-4, E3-2, E3-4
  conversion example E1-4, E3-11
  conversion procedure E3-6
  conversion requirements E3-4
  converting files E1-2, E3-1
  generic E3-5, E4-2
  importing files E4-5
  interconnections E3-15
  library component E4-2
  using in schematics E4-9
PAL interconnect report E3-10, F3-29
PALASM A1-1, A1-5, A7-4, A7-17, A8-2, E1-3, M5-17, U2-3, V16-34
PALCONVT A7-18
  accessing through XDM R1-25
PALCONVT command F2-26
PALCONVT menu
  command E3-2, E3-8
  verification E3-10
  example E1-8
palette command F2-40
  accessing through XDM R1-34
palettes.xct file R3-70
PAR partitioner report file F/ApC-22
PAR_IN
  SHIFT B4-94
PAR_OUT
  SHIFT B4-96
parallel ports
  XC3000 Demonstration Board H1-10
parameter file A6-40, R2-40, R2-187, R2-208, R2-217
paramfile option A6-40, R2-40, R2-208, R2-217
parity error V16-3, V16-44, V16-45
  elimination O16-52
part
  determining speed of F2-40
  family, selecting F2-17, F2-38
part attribute V4-11, V5-20, V11-94, V16-26, V/ApD-17
part command F2-40
  accessing through XDM R1-34
Part menu V5-20
part settings field F2-17
part type A6-8, A6-24, M10-20
  XNFPrep R2-41
PART, *see* PARTTYPE
partition log report A7-22
partition statement E2-16, E5-1, E5-26, F4-32
  example of F/ApC-19
  logical E5-3
  physical E5-3
Partition, Place, and Route program R1-5, R2-165
Partition, Place, and Route program *see* PPR
partitioner

report F/ApC-22
partitioner integrator module F5-5
partitioner log report A7-22, F3-22
partitioner report F3-9, V16-36
partitioning E4-2, U5-2
partitioning guide file R2-44
partitioning report E5-22
partitioning software O2-4
sample sdt.cfg file O2-4
partlist.xct file R2-124, R2-128
parttype attribute O4-9, O5-23
parttype option A6-8, A6-11, A6-24, A6-26, A6-40, A6-44, B/Ap-2, O10-8, R2-36, R2-41, R2-209, R2-217
path
statement for XDM F2-2, F2-4
path delays R2-166, R2-183, R2-195, R2-196, R2-200, R2-209, R2-215, R2-218, R2-219
combinatorial paths R3-9
ending points R3-6
flagging blocks R3-18
margin delays R3-18
searches R3-26
setting margin delays R3-17
setting maximum delays R3-13
setting minimum delays R3-13
starting points R3-6
worst-case R3-3
path types
clock–to–pad R1-86
clock–to–setup R1-86
pad–to–pad R1-86
pad–to–setup R1-86
path and XACT directory F/ApC-5
path_timing option R2-197, R2-209, R2-219, V4-10, V4-11
path–type timing specifications R1-85
basic path types R1-86
clock to pad R1-89
clock to setup R1-86
pad to pad R1-90
pad to setup R1-88
resolving conflicts R1-92
PBK file R2-45
PDS file E3-7, E4-3
PDS files F5-15
peripheral mode U6-13
peripheral synchronous mode U6-18
permutable inputs V/ApD-13
permute option V/ApD-13
permuteinputs option V/ApD-13
PGF file R2-43, R2-44, R2-45, R2-52, R2-168, R2-172, R2-177, V11-140, V11-144
Physical Interconnect Editor (PIE)
See also PIE R3-77
physical partition statements E5-3
PIC file R3-70
PIE R3-78
PINFBK pin option F4-18
pinlblsize option V/ApD-14
pinlist
report F3-7, F/ApC-21
pinlist report A7-22, E5-5, O16-39, V16-23, V16-36
pinlock flag O4-19
pinlock net attribute *see* P net attribute
pinout V14-11, V16-36
pins
adding to net in XDE R3-96
APR constraints R2-146
assigning nets in XDE R3-97
assignment E5-1, E5-2, F/ApC-22, O16-28
example O16-28
example of F/ApC-19
assignment (in PALCONVT) E3-2
assignment (precautions) E5-2
attribute O4-3
block type V/ApA-18
bus R2-14
changing functionality in XDE R3-188
clock R3-13

pins *(Continued)*
configuring interconnects in XDE R3-172
declaration statements A3-10, A3-16, A4-16, A7-6, A7-7, A9-20, A9-24
CEPIN F4-6
FASTCLOCK F4-10
FOEPIN F4-13
INPUTPIN F4-16
IOPIN F4-18
OUTPUTPIN F4-30
deconfiguring interconnects in XDE R3-191
deleting from nets in XDE R3-120
deleting in XDE R3-122
ending points for path delay in XDelay R3-6
equation F4-57
FastCLK F4-10
FastInput F4-12, F4-56
feedback E3-16, E3-17, E5-10
FOE F4-13
FOE option F4-19, F4-30
freezing F2-24, F2-25, F/ApC-20, F/ApC-22
grid arrays L1-67
I/O, defining F4-18
input source equation (PIN) F4-57
input, defining F4-16
invalid names R3-36, R3-37
keyword E5-2
labels V16-48
locations O11-54
moving net connection in XDE R3-148
moving window to in XDE R3-137
multiple connections to blocks R3-44, R3-45
multiple connections to net R3-36
names,report F3-7
options A6-28, A6-48
PINFBK option F4-18
pinlist report file F/ApC-21
PINTRST option F4-30
routing on block in XDE R3-172
setting constraint file flag in XDE R3-146
snapping to cursor in XDE R3-185
statements E3-2, V14-7
starting points for path delay in XDelay R3-6
swapping on matched blocks in APR R2-135
symbols in XNFMerge R2-6, R2-22
unrouting on blocks in XDE R3-191
usage report F3-5
pinsave
accessing through XDM R1-22
command E5-1, F2-18, F2-23, F/ApC-20, F/ApC-22, L1-21, V5-16
file E5-1, E5-3, V16-36
pins-format option A6-13
pin-to-block connections V4-12, V/ApD-18
pin-to-pin connections V4-12, V/ApD-18
pin-to-pin delay calculation E5-10
pintrst
pin option F4-19, F4-30
property A7-10
pintype attribute V4-12, V10-3, V11-36, V11-39, V11-96, V/ApE-11, V/ApE-18, V/ApE-22, V/ApE-23
pintype property M4-2
pipelining V15-10
PIPs U1-12, U9-27
snapping to cursor in XDE R3-185
PKG file
APR R2-144
PL20, using E4-2
PL20PIN V5-11, V5-15
PL20V8 V5-11, V5-15
PL22V10 V5-11, V5-15
PL24, using E4-2
PL24PIN V5-11, V5-15

PL48, using E4-2
PL48PIN V5-11, V5-15
PLA file A1-6, A1-8, A6-30
PLA option A6-45, A6-47
PLA2EQNX A1-6, A1-8, A1-12, A5-6, A5-7, A6-6, A6-35
place
  bus entry elements O11-29
  junction symbol O11-31
  labels O11-31
  module ports O11-33
  primitives O11-37
  stimulus and trace O12-6
  wires O11-30
place block constraint L1-49, R2-151
place constraints L1-51
place instance constraints L1-48, L1-55
place net constraint R2-152
place_effort option R2-191, R2-210, R2-218
place-and-route constraints A1-12
placement U1-15, U3-6
  place in design implementation R1-2
placer_effort option V10-11
PlaceRoute menu R1-23, V10-2, V11-126
PLASimX
  BL0 file A6-16, A6-31
  displaying signal list in simulation results A6-48
  functional simulation A1-1, A1-9, A9-26
  initializing registers A6-48
  initializing state machine A3-13, A4-2
  inputs A1-8
  options
    -break A6-48
    -initial A6-48
    -ivector A6-48
    -o A6-48
    -signal A6-48
    -trace A6-48
    -x A6-49
    -z A6-49
  output SM# file A1-8, A5-5, A5-6, A6-6, A6-35
  purpose A1-6
  running on command line A5-9, A6-47
  selecting simulation
    don't-care values A6-49
    high-Z values A6-49
    results format A6-48
    trace level A6-49
  simulating ABL file A5-4, A6-12, A6-34, A9-26
  specifying first and last vector number in results file A6-48
  specifying output file name A6-48
  specifying TMV file name A6-48
  test vectors A9-25
  TMV file A6-11, A6-14, A6-16, A6-29, A6-31, A6-34, A6-48
  viewing errors A6-19
PLC L1-30
PLD M1-1, M3-7, M5-1
  assembling equations for F2-22
  compilers F5-15, F/ApC-11
  development methods E4-4
  files E4-3, F5-15
  files, used in schematics E4-1
  library components E4-1
  linking symbols to schematic E4-8
  pin position labels F4-8
  state-machine design E1-3
  truth table input E1-3
PLD attribute A5-10, M5-17, V5-10, V5-13, V5-15
  architectures L1-37
  purpose L1-37
  syntax L1-37
PLD compilers
  ABEL E1-3
  ABEL XFER utility E3-7
  CUPL E1-3

PLD compliers *(Continued)*
CUPL -c option E3-7
LogIC E1-3
OrCAD PLD E1-3
third-party E1-3
using E4-4
XABEL E1-3
PLD equations
Boolean equations O16-31
define functions O16-30
equation file L1-38, M5-12, V5-10
processing JEDEC file O16-38
RCVR.ABL file O16-33
RCVR.PLD file O16-31
PLD file
converting from ABEL-HDL file A6-10, A6-33, A6-41, A7-18
merging with schematic A7-19
output from PLA2EQNX A1-8
Viewing equations A6-36
viewing equations A6-6
PLD functional simulation
dialog box M6-4
PLD symbols A7-5, A7-19, M3-10, V1-4, V5-1, V5-4, V5-10, V5-13, V5-14, V5-15, V6-1, V6-7, V7-10, V10-5, V10-13, V16-28
PLD timing simulation
dialog box M8-2
PLD XNF translation
dialog box M6-2
PLD= property M3-10
PLD_DA M1-1, M1-6
entering M2-5
see also Design Architect
PLD_DMGR M1-4
running applications M2-4
see also Design Manager
starting M2-3
PLD_DVE
Design Manager M1-6
dialog box M6-9
error messages M/Ap-7
functional simulation M10-5, M10-7, M10-8, M10-11
options M10-25
PINTYPE property M4-2
syntax M10-25
variables M10-25
PLD_DVE_BA M10-15
error messages M/Ap-6
options M10-26
syntax M10-26
variables M10-26
PLD_DVE_SIM M10-3
error messages M/Ap-7
functional simulation M10-5, M10-7, M10-9, M10-11
options M10-27
syntax M10-26
timing simulation M10-15, M10-17, M10-18
variables M10-26
PLD_FNCSIM8 M1-2, M1-6, M6-1, M6-4, M6-6
See also FNCSIM8
see also functional simulation
PLD_Men2XNF8 M1-6, M6-1, M7-1, M11-83
output files M11-84
see also Men2XNF8
PLD_TIMSIM8 M1-2, M1-7, M8-1
see also timing simulation, TIMSIM8
PLD_XDM M1-7
PLD_XEMake M1-2, M1-7, M7-1, M7-5
dialog box M7-5
MAK file M7-6
output files M7-7
see also XEMake
target file M7-6
PLD_XMake M1-2, M1-7, M7-1, M11-85
dialog box M7-1
output files M7-7, M11-87

See also XMake
target file M7-4
PLFB9 L1-33, V5-11, V5-15, V5-21
using E4-3
PLFB9 keyword E4-3
PLFFB9 V5-11, V5-15, V5-21
using E4-3, E4-13
PLFFB9 keyword E4-3
PLO L1-30, L1-59
Plot menu V/ApA-35
plot-go command V/ApA-35
PLUSASM A5-2, A7-1, E1-2, L1-37, L1-38, M3-10, M5-1, M5-12, M10-13
accessing from XDM R1-22
assembler
partitioner and minimizer F5-5
assembly-log report A7-22, A7-23
AUTHOR keyword V16-29
CHIP keyword V5-13, V5-15, V16-29
command A7-23, F2-22
overview F4-1
COMPANY keyword V16-29
COMPONENT keyword V5-13, V5-15
converting ABL file A7-17
converting JEDEC file A7-5, A7-21
creating designs E2-1
DATE keyword V16-29
declaration section E2-3, F4-4
definition A1-1
delimiters F4-68
equation files F5-15
equation files *see* equation files
equation modules A7-3, A7-20
equations A1-6, O5-13, O16-31
EQUATIONS keyword V16-29
equations section E2-4
errors and warnings V16-35
file structure E2-2, F4-2
files, equation section F4-40
header section E2-2
include_eqn statement A7-4, A7-18, A7-20
inclusion in multiple-file design A7-4, A7-17
INPUTPIN A7-6
IOPIN A7-6
mixing with ABL files A1-5
naming file with module statement A3-10
nodetrst statement A7-10
operators and special characters F4-68
OUTPUTPIN A7-6
pintrst statement A7-10
PLD attribute M5-17
PRLD equations V5-20
property statement A1-5, A1-11, A7-2, A7-4, A7-6, A7-7, A7-9, A7-15, A7-20, A9-37
reserved characters F4-69
running with XEMake V7-10, V16-33
syntax F4-72
text files V16-10
TITLE keyword V16-29
top-level file A7-18
user-defined primitives M5-14
using E4-4
XEMake A1-12
polarity A4-5, A6-11, A6-27, A7-14, A7-15, A/ApB-1, A/ApB-2
of signals, defining F4-66
polarity conflicts
resolving with PALCONVT E3-2
port components
design rules F5-8
pos attribute A4-6, A6-11, A6-27, A7-14, A7-15, A7-16
Postscript R3-77
power regulator
XC4000 Demonstration Board H2-1, H2-2
power switches
XC4000 Demonstration Board H2-11

power-on reset F4-58
power–up
  reset B2-9
Powerview V1-1, V1-2, V2-1, V11-3, V12-3, V12-49
PPR M1-8, M9-3, R1-39, R1-40, R3-29, U3-2, U5-4
  accessing through XDM R1-24
  BUFT constraints L1-67
  changing routing from guide file R2-178, R2-183, R2-195, R2-207, R2-220
  CLB constraints L1-63
  completing placement but not unguided routing R2-182, R2-195, R2-203, R2-220
  considering path delays in placement and routing R2-197, R2-209, R2-219
  constraints R2-185
  constraints file V11-116
  controlling placement quality and time R2-192, R2-210, R2-218
  controlling routing quality and time R2-192, R2-212, R2-218
  copying routing from guide file R2-194, R2-203, R2-220
  creating LCA file V10-5
  critical nets V4-10
  CST file R2-184, R2-190, R2-220
  default path timing V15-9, V15-22, V15-38
  defining pinout V11-95
  design flow
    default R2-165
    XC3000A/L with X-BLOX R2-172
    XC3000A/L without X-BLOX R2-168
    XC3100A with X-BLOX R2-172
    XC4000 with X-BLOX R2-170
    XC4000 without X-BLOX R2-167
  detecting combinatorial logic loops V11-121, V15-32
determining blocks to be guided R2-185, R2-194, R2-202, R2-219
devices supported V11-143
displaying list of options R2-204, R2-217
edge decoder constraints L1-69
families supported R2-165
FILE attribute V4-3
FMAP mapping L1-59, L1-60
forward tracing mechanism R1-93
generating device utilization statistics R2-189, R2-202, R2-217
global buffer constraints L1-70
guide file V11-139, V11-144
guided design R2-175
  constraints R2-184
  incremental design R2-175, R2-179
  iterative design R2-175, R2-178, R2-179
  obtaining best results R2-176
  options R2-178
  placement and routing in XDE R2-175, R2-180
  PPR and APR R2-184
  XACT-Performance specifications R2-183
  XC3000A/L designs R2-177, R2-184
  XC3100A designs R2-184
  XC4000 designs R2-177
guiding design implementation R2-184, R2-194, R2-202, R2-219
HMAP mapping L1-59, L1-60
I/O constraints L1-64
ignore_maps option L1-59
ignore-xnf_locs option L1-20
ignoring FMAP/HMAP symbols R2-184, R2-191, R2-205, R2-217
ignoring LOC constraints R2-184, R2-191, R2-206, R2-217

PPR *(Continued)*
ignoring RLOC constraints R2-184, R2-191, R2-205, R2-217
ignoring XACT-Performance requirements R2-197, R2-206, R2-219
INIT attribute V4-4
input files R2-174
CST R2-174
LCA R2-174
MAP R2-165, R2-174
XTF R2-165, R2-174
interaction with XACT-Performance V15-10, V15-13, V15-23
invoking
command line R2-186
XDM R2-186
IOB constraints L1-67
LCA file V10-15, V15-9, V15-25
LOC constraints L1-55, L1-57
log file O15-30, O15-41, R2-174, V15-9, V15-22, V15-23, V15-24, V15-25, V15-30, V15-39
meeting XACT-Performance requirements R2-197, R2-214, R2-219
naming constraints file R2-190, R2-198, R2-217
net absorption V4-10
options
complete R2-190, R2-198, R2-217
cstfile R2-190, R2-198, R2-217
dc2p R2-196, R2-198, R2-218
dc2s R2-196, R2-199, R2-218
dflt_sig_dly R2-197, R2-200, R2-218
dp2p R2-196, R2-200, R2-219
dp2s R2-201, R2-219
estimate R2-189, R2-202, R2-217
guide R2-167, R2-168, R2-170, R2-172, R2-177, R2-184, R2-194, R2-202, R2-219
guide_blks R2-178, R2-180, R2-181, R2-182, R2-185, R2-194, R2-202, R2-219
guide_only R2-178, R2-182, R2-195, R2-203, R2-220
guide_routing R2-178, R2-180, R2-182, R2-194, R2-203, R2-220
guide_thru_routes R2-178, R2-180, R2-182, R2-183, R2-195, R2-204, R2-220
helpall R2-204, R2-217
ignore_maps R2-184, R2-191, R2-205, R2-217
ignore_rlocs R2-184, R2-191, R2-205, R2-217
ignore_timespec R2-197, R2-206, R2-219
ignore_xnf_locs R2-184, R2-191, R2-206, R2-217
lock_routing R2-178, R2-180, R2-182, R2-183, R2-195, R2-207, R2-220
logfile R2-189, R2-207, R2-217
outfile R2-175, R2-189, R2-208, R2-217
paramfile R2-208, R2-217
parttype R2-209, R2-217
path_timing R2-197, R2-209, R2-219
placer_effort R2-191, R2-210, R2-218
route R2-210, R2-218
route_thru_blks R2-193, R2-211, R2-218
route_thru_bufg R2-193, R2-211, R2-218
router_effort R2-192, R2-212, R2-218
rpt_net_loc R2-213, R2-219
rpt_sym_loc R2-213, R2-219
save_files R2-213, R2-217
seed R2-214, R2-218

PPR options *(Continued)*
stop_on_miss R2-197, R2-214, R2-219
timing R2-192, R2-215, R2-218
use_faster_c2s R2-196, R2-215, R2-219
user_search_path R2-216
output files R2-174
LCA R2-174, V7-1
LCB R2-174
LOG R2-174
RPF R2-174
RPT R2-174
parameter file R2-187
path analysis R2-29
path_timing option V4-10, V4-11
place block constraints L1-49
place instance constraints L1-48
placement constraints L1-46
constraints file syntax L1-47
schematic syntax L1-46
placer_effort option V10-11
preserving through-routes R2-178, R2-183, R2-195, R2-204, R2-220
printing summary of net locations R2-213, R2-219
printing summary of symbol locations R2-213, R2-219
processing hard macros R1-111, R1-114, R1-116
purpose R1-5, R2-165
renaming log file R2-189, R2-207, R2-217
renaming RPT and LCA files R2-189, R2-208, R2-217
report file V11-12, V11-119, V11-124
RLOC constraints L1-71
route option V10-11
routing design R2-193, R2-210, R2-211, R2-218
routing through global buffers R2-193, R2-211, R2-218
RPT file R2-166
running in XMake R2-187
running with XMake V7-6, V7-11, V7-12, V13-20, V14-23
saving temporary files R2-213, R2-217
specifying default
clock-to-pad time R2-196, R2-198, R2-218
clock-to-setup time R2-196, R2-199, R2-218
pad-to-pad time R2-196, R2-200, R2-219
pad-to-setup time R2-201, R2-219
specifying maximum delay target R2-197, R2-200, R2-218
specifying options in parameter file R2-208, R2-217
specifying search path R2-216
specifying seed R2-214, R2-218
specifying target LCA device R2-209, R2-217
specifying timing information for router R2-192, R2-215, R2-218
specifying whether design is complete R2-190, R2-198, R2-217
suspending routing R2-187
timing analysis summary V15-25
timing attributes V4-9, V15-1
timing specifications R1-69
tracing paths through Set and Reset pins V15-30
tying unconnected input pins to default value R1-111
use with DOUBLE attribute L1-12
using faster C2S specification R2-196, R2-215, R2-219
warnings V11-121, V15-24
weight net attribute values L1-34
X net attribute L1-35
xactinit.dat files R2-188

PPR *(Continued)*
XACT-Performance specifications R2-166
preamble U6-22
precision B2-17
predefined groups R1-72
preload
initialization M9-3
preload equation (PRLD) F4-58
preload register E2-11, E2-15, E5-26
preload register (XC7336) E2-16
PRELOAD_OPT M9-4
PRELOAD_OPT attribute O5-22, V5-19, V9-6, V16-26
architectures L1-38
purpose L1-38
syntax L1-38
PRELOAD_OPT property M5-17, M5-21
pre-synthesis logic-reduction option A6-8, A6-24
prg files F5-16, F/ApC-22, M7-7, M10-13, O10-15, V7-1, V7-10, V7-12, V10-13
primary directory V2-5
primitives U2-1
CLB V4-5, V6-7, V6-11, V10-5, V10-6, V10-9
CLBMAP V4-10
definition V3-4, V11-77
description O11-45
EPLD M5-13, V5-12
user-defined M5-14
EPLD attributes V5-15
FPGA M3-4
grouping symbols with TNM V15-6
IOB V4-3, V4-5, V4-10, V4-14, V6-7, V6-11, V10-5, V10-6, V10-9, V10-10
LEVEL attribute V11-82
library V11-80
macro V15-5
PINTYPE attribute V4-12
placing primitives O11-37
supplied by Xilinx O4-2
symbols R2-5, R2-10
user-defined V5-12
primitives and macros
XC4000 library exceptions
power and ground symbols O4-20
printcap.xct file R3-73, R3-75, R3-158
printer command F2-40
PRLD
equations F4-58, L1-38, M5-22, V5-20
forcing M9-5
initialization M9-3
signals O10-22, V9-5, V9-8, V16-41
PRO capture V1-1, V1-2
PRO file V11-115
PRO Series V1-1, V1-2, V2-1, V11-3, V12-3
probes U4-10
assigning nets R3-97
printing list in XDE R3-166
reading into LCA file in XDE R3-169
saving to PRB file in XDE R3-176
product terms A6-47
clock E3-17
exported E5-2
partitioner and minimizer F5-4, F5-6
shared E5-23
Profile menu F2-17, F2-38, R1-9, R1-19, R2-274
command E3-7
saveprofile command V11-115, V11-116
XDM R1-32
profile options
APR command V11-116
command V11-144
XMake command V11-115
XNFPREP command V11-116
profile-family command A5-1
profile-keydef command V16-10, V16-39
profile-part command A5-1
profile-speed command A5-1

PROgen V1-1, V1-2
proglist.xdm file F2-1, F2-6, R1-8, R1-14
PROGRAM U8-4, U8-9
program command
  XPP H4-19
program list file F2-1
program options
  SDT2XNF O/ApA-1
  XDraft O/ApA-1
  XNF2VST O/ApA-2
program push button
  XC3000 Demonstration Board H1-5, H1-14
  XC4000 Demonstration Board H2-2
programmable interconnect points *see* PIPs
Programmable Logic Arrays (PLAs) A4-5, A4-16, A8-1
Programmable Logic Device M1-1
programming (device) E1-11, E3-9, E4-9
programming file F5-16, F/ApC-22
  MAKEJED (JEDEC) O16-41
  MAKEPRG (hex format) O16-41
programs
  *see also* XSimMake, XMake, XEMake
  ASCTOVST O10-25
  INET O10-5
  INF2XNF O10-7
  MemGen O4-21
  SDT2XNF O10-7
  Symgen O4-21
  XDraft O2-8
  XNF2INF O10-19
  XNF2VST O10-19
  XNFMerge O10-9
prohibit-block constraint R2-152
prohibit-location constraint R2-153
project-create command V2-3
project directory V2-2, V2-3, V2-4, V2-5, V11-6, V11-7, V11-23, V12-5, V12-9, V12-29, V13-2, V14-2, V16-12
  configuration O11-5
  creation O11-5
projectp-search-viewdraw command V2-7
project-create command V11-23, V16-12, V16-47
project-search-Viewdraw command V16-12
PROLINK M1-2, V16-37
  accessing through XDM R1-27
  command F2-33, F/ApC-22
  download program A7-21
PROM R1-5, R2-270, U1-13, U6-6,V11-134
  DIP switches H1-12
  files U6-3, V7-1
    image R2-270
  formats
    EXORMAX H4-2, R2-270, R2-271, R2-274, R2-278, R2-281
    MCS–86 H4-2, R2-270, R2-271, R2-274, R2-275, R2-278, R2-279, R2-281
    TEKHEX H4-2, R2-270, R2-271, R2-274, R2-278, R2-281
  FPGA Demonstration Board H3-25, H3-27
  hex files
    XC3000 Demonstration Board H1-14
  LCA configuration
    XC3000 Demonstration Board H1-13
  menu R2-274
  module B4-2, B4-84
    BOUNDS B4-86
    Default Radix=Hexadecimal B4-90
    Definition Procedure B4-90
    DEPTH B4-85
    ENCODING B4-85
    MEMFILE B4-85
    TNM B4-86
  reset H1-13
  serial configuration

PROM *(Continued)*
XPP H4-1
sockets
XC4000 Demonstration Board H2-13, H2-15
XC3000 Demonstration Board H1-9
XC4000 Demonstration Board H2-1, H2-2
XChecker H5-8
XPP H4-2
properties L1-2, M3-7
add or modify FPGA M4-1
adding M3-7
EPLD M5-15
adding M5-16
CLOCK_OPT M5-21
FOE_OPT M5-21
global M5-16
LOC=pin_name M5-18
LOGIC_OPT M5-20
LOWPWR M5-19
MINIMIZE M5-20
MRINPUT M5-23
NETFLAG M5-22
OPT M5-19
PLD=file_name M5-17
PRELOAD_OPT M5-21
REG_OPT M5-21
UIM_OPT M5-20
FPGA M4-1
BASE M4-9
BLKNM M4-3, M4-4
CAP M4-9
CMOS M4-9
COMP M4-1, M4-2
CONFIG M4-10
DECODE M4-4
DOUBLE M4-4
EQUATE_F M4-10
EQUATE_G M4-10
FAST M4-8
FILE M4-2
HU_SET M4-8
INIT M4-5
INST M4-2
INTERNAL M4-8
LOC M4-6
MEDFAST M4-9
MEDSLOW M4-9
NET M4-13
NETFLAG M4-13
NODELAY M4-8
PINTYPE M4-2
REF M4-1
RES M4-9
RLOC M4-7
RLOC_ORIGIN M4-8
RLOC_RANGE M4-8
SLOW M4-8
TNM M4-11
TSidentifier M4-11
TTL M4-9
U_SET M4-7
USE_RLOC M4-7
modifying M3-8
see also specific property.
property statement A7-2, A7-4, A7-6, A7-7, A7-9, A7-15, A7-20
PROsim V1-1, V1-2
PROsynthesis V1-1, V1-2
PROwave V1-1, V1-2
PRP file M7-8, O11-76, R2-32, R2-41, V11-119, V11-120, V13-13, V13-17, V13-20, V15-24
Prtsc key R3-131
PRX file R2-32, R2-41
PUC L1-30, L1-59
pulldown transistors L1-6, L1-40
pullup resistors L1-11, L1-12, L1-20, R2-10, R2-127, R3-34, R3-35
3-State B4-111
XC3000 Demonstration Board H1-6

PULLUP symbols L1-11, L1-20, V4-4, V4-5, V11-110
PULLUP_D resistor
3-State B4-111
pulse-width modulator example E2-4
PUO L1-30, L1-59
PWR statement F4-38
PWRDN V3-2

## Q

Q_OUT
ACCUM B4-11
COUNTER B4-38
DATA_REG B4-50
QueryNet U4-8
query-template option V15-28, V15-31
QuickPart tables M9-1
QuickPath M1-5, M8-6
dialog box M8-6
QuickSim II M6-6, M9-1
analyzing nets M9-1
dialog box M6-7, M8-4
functional simulation M6-1, M6-7
Icon M1-5
options M10-27
simulation models M9-1
syntax M10-27
timing simulation M8-1, M8-3
tutorial M12-1
adding traces manually M12-12
asserting global reset M12-15
asserting global set reset M12-16
assigning values to clock M12-13
command file M12-28
command summary M12-29
design description M12-17
do file M12-29
FNCSIM8 M12-29
functional simulation M12-6
installing M12-4
Men2XNF8 M12-29
opening list window M12-10
opening trace window M12-10
PLD_FNCSIM8 M12-7
PLD_Men2XNF8 M12-7
PLD_TIMSIM8 M12-27
required software M12-2
saving waveform data M12-24
selecting nets for simulation M12-8
simulating the circuit M12-18
timing simulation M12-27
timsim8.log file M12-28
using the transcript M12-26
viewing calc schematic M12-7
variables M10-27
quiet option V/ApD-8
quitting XDM F2-3, F/ApC-6

## R

r option A6-42, R1-113, R1-114, R1-117, R1-118, R1-119
radix V/ApB-8, V/ApB-15, V/ApC-14, V/ApC-15, V/ApC-18, V/ApC-26
Radix menu V/ApC-14
radix-binary command V/ApC-14
radix-decimal command V/ApC-14
radix-hexadecimal command V/ApC-15
radix-octal command V/ApC-14
RAM constraints L1-57
RAM16X1 L1-72
RAM32X1 L1-72
RAM64X8 L1-57, L1-58
RAMs A1-13, L1-42, M4-5, O4-21, R1-3, R1-61, R1-62, R1-64, R2-170, R3-19, R3-139, V1-2, V3-9, V4-5, V4-9, V4-14, V6-11, V11-105, V11-106, V12-19, V12-40, V15-4, V15-5, V15-14, V15-15, V/ApB-23, V/ApB-24
created by MemGen R1-59
RAMs set V15-6, V15-7, V15-8, V15-15, V15-17, V15-19
rawbits file R2-228

RBT file R2-229
MakeBits R2-228
RC relaxation oscillator
XC3000 Demonstration Board H1-4, H1-8
RCLK modifier E2-7, E2-8
RCVR.ABL file, contents F/ApC-14, O16-33
RCVR.PDS file, contents F/ApC-12
RCVRSUB schematic O16-60
read command
XPP H4-21
ReadAbort U7-12
readback U7-1, U8-18
bitstream U7-4, U7-9, U7-10
daisy chain U7-4
during boundary scan U7-9
features U7-2
frequency U7-13
initialization U7-8
options U7-12
performing U7-5
pins U7-7
ReadAbort U7-12
ReadCapture U7-12
ReadClk U7-12
state flow diagram U7-5
switching characteristics U7-14
symbol U7-8
timing U7-13
uses U7-2
within XDE U7-9
readback (XC4000)
capture flip-flops R2-249
enable/disable abort capability R2-249
readback clock source R2-249
readback enable/disable
XC3000 R2-247
readback primitive U7-6, U7-8
readback symbol U7-8, U8-18
ReadCapture U7-12
ReadClk U7-12
read-only directory V2-5
readprofile command F2-40
accessing through XDM R1-34
read-template option V15-28, V15-31
read-write directory V2-5
recycled aliases O10-24
reduce option A6-47
reduction A7-14
REF property M4-1
reference designators, updating F2-20
reg attribute A4-6, A7-14
reg keyword A3-16
reg_d attribute A4-6, A7-14
reg_g attribute A4-6, A7-14
reg_jk attribute A4-6, A7-14
reg_opt attribute O5-22, V5-8, V5-19
architectures L1-39
purpose L1-39
syntax L1-39
reg_opt property M5-17, M5-21
reg_sr attribute A4-6, A7-14
reg_t attribute A4-6, A7-14
register
register clock source (CLKF) F4-48
register functions, see Xilinx Libraries Guide for description and selection details
register L1-36, L1-38
data storage B4-2
initialization A6-14, A6-48
optimization F5-9
ordering
OrCAD/SDT R2-51
XNFMAP R2-50
powerup 0 option A6-14
powerup 1 option A6-14
preload E2-11, E2-15, E5-26
preload (XC7336) E2-16
shift B4-2
simulation values A6-30

registered equations E2-10, E2-15, E3-18
asynchronous clear E2-11
asynchronous set E2-11, E4-13
using FastCLK E4-13
registered inputs E2-8
registered logic A3-12, A9-21, A/ApB-1
register-powerup-state option A6-30
register-simulation values A6-14
relationally placed macro
see RPM
relationally placed macro, *see* RPM
relationally placed macros L1-72, L1-96, R1-111, R2-11, R2-12, V1-3, V3-4, V6-8, V11-77, V11-83, V11-86
relative location constraint R1-111
Release 5.0
new features O1-3
SDT2XNF enhancements O1-5
XNF2VST enhancements O1-5
release command V/ApB-18
Release menu V/ApB-18
removing files F2-34
REP file A1-8, A6-6, A6-35
repeating commands A6-5, F2-9
report command
accessing through XDM R1-31
report files F5-15, F/ApC-21, M7-8
report option R2-36, R2-41
reports
APR R2-156
EQN file F3-33
equation report E5-5, E5-8
logic optimizer F3-16
mapping F3-4, F/ApC-21
optimized outputs F3-17
PAL interconnect F3-29
PAL interconnect report E3-10
partitioner F3-9, F/ApC-22
partitioner log F3-22
partitioning report E5-22
pinlist F3-7, F/ApC-21, O16-39
pinlist report E5-5
pins and product term allocation F3-22, F3-23
resource F3-2, F/ApC-21
resource report E5-5, E5-8
viewing F3-1
RES attribute O4-16, V4-8
architectures L1-39
purpose L1-39
syntax L1-40
RES property M4-9
RES resource report file F/ApC-21
reserved names V3-2
reset push button
XC3000 Demonstration Board H1-5
XC4000 Demonstration Board H2-2
reset signals
XC2000/3000 families O12-19
XC4000 family O12-19
reset switches
XC4000 Demonstration Board H2-12
reset timing
XC3000 R2-247
resistive mode L1-6, L1-39, V4-8
resistors
pulldown B2-12
pullup B2-12, L1-11, L1-12, L1-20, R2-10, R2-127, R3-34, R3-35
resource report A7-22, E5-5, E5-8, V16-35
resources
munching unused F5-3
restart option V/ApD-8, V/ApD-14
retain option A6-46
retargeting design M2-6, O2-15
example O2-17
revision statement E2-3
RIGHT_LEFT
SHIFT B4-95
rip U7-7
rip component M3-5
RIPPLE attribute B4-12, B4-16, B4-66

RIPPLE style B4-34, B5-3
RISING R1-79
RLOC attribute O4-16
RLOC constraint L1-18, R1-111, R1-113, R2-184, R2-191, R2-205, R2-217, V4-6, V11-85
  architectures L1-40
  carry logic L1-99
  ignoring in XNFPrep R2-38
  propagation L1-94
  purpose L1-40, L1-71
  set linkage L1-78
  set modification L1-80
  set modifiers L1-85
  sets L1-74, L1-94
  symbols L1-72
  syntax L1-40, L1-46, L1-72
  use with pre-unified libraries elements L1-72
  use with unified libraries elements L1-72
  use with Xilinx macros L1-93
RLOC parameters R2-12
RLOC property M4-7
RLOC_ORIGIN attribute B5-3, O4-16, R1-113
  ACCUM B4-12
  ADD_SUB B4-16
  COUNTER B4-41, B4-112
  DATA_REG B4-51
  INC_DEC B4-66
  Restrictions B6-10
  SHIFT B4-98
RLOC_ORIGIN constraint L1-72, L1-91, V4-6
  architectures L1-41
  modifying H_SET L1-87
  modifying HU_SET L1-87
  purpose L1-41, L1-86
  syntax L1-41, L1-86
RLOC_ORIGIN property M4-8
RLOC_RANGE attribute B5-4, O4-16
  ACCUM B4-12
  ADD_SUB B4-16
  COMPARE B4-34
  COUNTER B4-42
  DATA_REG B4-51
  INC_DEC B4-66
  Restrictions B6-10
  SHIFT B4-99
RLOC_RANGE constraint V4-6
  architectures L1-42
  purpose L1-42, L1-89
  syntax L1-42, L1-90
RLOC_RANGE property M4-8
rocker switches V11-136
ROM O4-21
  INIT property M4-5
  simulation M9-3
ROM constraints L1-57
ROM16X1 L1-72
ROM32X1 L1-72
ROMs A1-13, L1-18, R1-3, R1-61, R1-64, R2-170, V1-2, V1-4, V3-9, V4-4, V4-14, V6-11, V11-106, V12-19, V/ApB-23, V/ApB-24
  bus representation style R1-59
  created by MemGen R1-59
  data values
    binary R1-62
    decimal R1-62
    hexadecimal R1-62
    octal R1-62
  initialization value R1-59
  setting default values in XDE R3-178
  unspecified locations R1-62
  XChecker H5-8
route option R2-210, R2-218, V10-11
route_thru_blks option R2-193, R2-211, R2-218
route_thru_bufg option R2-193, R2-211, R2-218

routed_only setting R2-181, R2-203
guide_blks option R2-185
router_effort option R2-192, R2-212, R2-218
routing U1-15, U3-7
manual via XDE U9-33
place in design implementation R1-2
routing resources U1-9, U9-28
direct interconnect U1-10
general purpose interconnect U1-11
longlines U1-10
PIPs U1-12
switch matrices U1-12
RPF file
output by PPR R2-166, R2-174
RPM B5-1, B6-2, B6-6, L1-72, L1-96, M1-8, M3-4
Aligned B4-12, B4-16, B4-66
Controlling RPM placement B5-3
converted from Xilinx-created hard macros R1-114
converting hard macros O1-4
definition R1-111
description O4-2, O11-45
error in converting R1-119
logic trimming R1-111, R1-112
RLOC_ORIGIN constraint R1-113
unaligned B4-12, B4-16, B4-66
unified libraries R1-114
view O11-47
RPMs *see* relationally placed macros
RPT file M7-8, O11-80, V11-12, V11-119, V11-124
APR R2-156
output by PPR R2-166, R2-175
rpt_net_loc option R2-213, R2-219
rpt_sym_loc option R2-213, R2-219
RST V3-2
RSTF equation F4-48, F4-59
rules for XEPLD designs F5-7
device-specific components F5-7
FastCLK, CE, and FOE F5-8
hanging inputs F5-7
port components F5-8
run command V/ApB-18
Run menu V/ApB-18

## S

S flag R2-8
S net attribute L1-34, V4-10
sample/preload U8-7, U8-11, U8-13, U8-16
save
drawing O11-36, O16-29
fill, changing file name O11-44
pin assignments O16-40
save command V11-52, V11-111, V/ApB-24
save flag O4-19
save net attribute *see* S net attribute
save_files option R2-213, R2-217
saveprofile command F2-40, V11-116
accessing through XDM R1-34
savesig option R2-35, R2-41, R2-190
save-template option V15-31
saving XDM settings F2-40
ScanDisk command
accessing through XDM R1-31
SCH file O3-8, V3-8, V10-27, V11-52, V12-8
sch subdirectory V2-2, V3-8, V6-2, V8-2, V11-6, V11-9, V11-52, V12-29, V/ApE-14
schematic
attributes E4-12
creating M3-6
design entry R1-2
editor O16-10
invoking Draft O2-15
entry U1-15, U2-1
MemGen U2-2
X-BLOX U2-2
file O3-8
integrating designs F2-25
reading netlists F5-3
schematic capture overview F1-7
specifying timing requirements R1-4

SCP
XC3000 Demonstration Board H1-13
SCP file
APR R2-143, R2-145
Map2LCA R2-108
SDT
exiting O11-68
software installation O2-2
sdt.cfg file O11-6
sample file O2-10
SDT2NET command F2-21, F5-15
SDT2XNF
accessing through XDM R1-22
SDT2XNF program
enhancements O1-5
error messages O/ApB-2
options O10-7
program options O/ApA-1
syntax O10-7
warning messages O/ApC-2
search path R2-216
searching a design file
in XPP H4-26
SEE file V9-9, V9-10, V12-28, V16-40, V/ApC-1, V/ApC-12
seed R2-214, R2-218
seed option R2-214, R2-218
SEL
MUXBUS B4-72
MUXBUS2 B4-74
MUXBUS4 B4-76
MUXBUS8 B4-78
SEL_ERROR
DECODE B4-59
MUXBUS B4-73
MUXBUS2 B4-75
MUXBUS4 B4-77
MUXBUS8 B4-79
SEL1 U8-10
SEL2 U8-10
Select menu V/ApA-29
select-attr command V/ApA-30
select-comp command V/ApA-31
select-group command V/ApA-32
select-label command V/ApA-29
select-name command V/ApA-30
SelectSpec option V15-28, V15-33
select-unselect command V/ApA-31
sequencer A9-18
sequential search order V2-5
serial configuration PROM programmer
XPP H4-1
serial ports
XC3000 Demonstration Board H1-10
XC4000 Demonstration Board H2-2
serial slave mode
FPGA Demonstration Board H3-26
XC4000 Demonstration Board H2-14
serial-in/serial-out
BUS_DEF B4-23
set (asynchronous) E2-11
setconfigset command
MakeBits R2-268
SETF equation F4-48, F4-60
set-project command V2-4, V11-25, V16-12, V16-47
set-reset flip-flops A4-15
settings
mouse button F/ApC-8
saving F2-40
settings command F2-40
accessing through XDM R1-34
settings fields F2-17
setup and hold timing calculation E5-13
setup command V2-2, V3-8, V11-7, V11-16
XPP H4-21
setup menu V/ApB-1
setup program V2-14
setup time V4-7, V9-3
setup time calculation E5-9
setup violations V9-3, V9-6
setup-breakpoint command V/ApB-8

setup-clock command V/ApB-7
setup-defaults command V/ApB-11
setup-logfile command V/ApB-11
setup-pattern command V/ApB-6
setup-radix command V/ApB-8
setup-stepsize command V/ApB-7
setup-trace command V/ApB-10
setup-vector command V/ApB-2
setup-vwave command V12-14, V/ApB-2
setup-watch command V/ApB-10
setup-waveform-aperiodic command V/ApB-3
setup-waveform-decrement command V/ApB-3
setup-waveform-increment command V/ApB-4
setup-waveform-multiply command V/ApB-5
setup-waveform-periodic command V/ApB-6
seven-segment displays
  XC3000 Demonstration Board H1-4, H1-7
  XC4000 Demonstration Board H2-1, H2-2, H2-10
shape of cursor, changing F2-38
sheet option V/ApD-8, V/ApD-9
sheet size V10-26, V16-15, V/ApA-20, V/ApD-8, V/ApD-9, V/ApD-16
sheet symbols V10-25
  attributssetup-Vwave-command V12-14etup-Vwave-command V12-14es V10-26
  contents V10-26
  copying O11-24
  defining O11-22
  definition O3-7
  global attributes V5-17
  lower-level schematic O16-59
sheet-path part O3-7
sheetsym option V/ApD-9
shell for XEPLD software F2-1
shelltool option A6-32
shift equation F4-61
shift module B4-92
  ASYNC_VAL B4-97
  BOUNDS B4-98
  ENCODING B4-97
  LOC B4-98
  parallel-in/serial-out B4-100
  register B4-2
  right/left control B4-95
  RLOC_ORIGIN B4-98
  RLOC_RANGE B4-99
  serial-in/parallel-out B4-99
  serial-in/serial-out B4-100
  STYLE
    ARITH B4-97
    CIRCULAR B4-97
    LOGICAL=Default B4-97
  SYNC_VAL B4-97
  TNM B4-99
  USE_RLOC B4-98
shift register functions, see Xilinx Libraries Guide for description and selection details
SHM4000 library V2-6, V2-12, V6-8
shortcuts for command entry F2-9
Show menu A6-34
show-any-file command A5-7, A6-36
show-compiled-equations command A5-7, A6-35
show-compiler-listing command A5-7, A6-35
show-error-log command A5-3, A5-6, A6-36
show-simulation-results command A5-5, A5-6, A6-34, A6-35
show-transcript command A5-6, A6-36
show-Xilinx-EPLD-equations command A5-7, A6-36

show-Xilinx-SYNTHX-report command
A5-6, A6-35
signal aliasing B2-22
signal attributes O4-5, O5-23
applicable devices O4-18
critical O4-18
external O4-19
G output O4-18
I input O4-18
K output O4-18
L net O4-18
non-critical O4-19
pinlock O4-19
save A1-11, O4-19
table of O4-18
TNM O4-19
TS O4-19
weight O4-19
signal binding R2-2, R2-6
by pin name R2-8
by signal name R2-7
signal option A6-15, A6-29, A6-30, A6-48
signals
active low F4-66
adding O16-28
defining polarity F4-66
guided routing R2-181
Signals menu V/ApC-5
signals-add command V/ApC-5
signals-copy command V/ApC-8
signals-create command V/ApC-7
signals-delete command V/ApC-7
signals-fromsch command V/ApC-6
signals-remove command V/ApC-6
signals-rename command V/ApC-8
signals-scroll command V/ApC-9
signals-select command V/ApC-9
signature M7-7
specifying for programming files
F2-31, F2-32
silent option A6-46
sim command V/ApB-19
Sim menu V/ApB-19
sim option B/Ap-2
SIMDIR M10-7, M10-11, M10-29, M13-10
simdir option B/Ap-2
simulate-options dialog box A6-28
simulate-trace-options dialog box A6-13
simulation
Functional A6-32
simulation E4-9, E5-3, R1-3, U1-15, U4-3
*see also* functional & timing simulation
automatic file creation F2-28
board-level designs E5-4
configuring VST (functional) O12-18
configuring VST (timing) O12-30
creating model for F/ApC-23
don't-care values A6-14, A6-30, A6-49
EPLD designs O16-41
device initialization O9-5
High-Z O9-6
PRLD O9-5
run simulation O6-6, O8-6, O16-48
trace file O16-47
view results O16-49
VST configuration O16-43
example A9-22
first vector in results file A6-15
FPGA designs
commands O12-24
globalreset buffer O9-1
globaltristate buffer O9-1
high-impedance inputs O9-2
hold violations O9-3
large ROMs in XC4000s O9-5
oscillators O9-3
pulse-width O9-2
run simulation O6-6, O8-6
time units O9-2
traces and stimuli O9-2
unconnected inputs O9-1
weak-keeper O9-2

simulation *(Continued)*
functional A1-1, A1-9, A5-4, A6-6, A6-12, A7-23, A9-22, B3-8, U4-4
guidelines O9-1
high-impedance values A6-14, A6-30
initialization state A4-2
last vector in results file A6-15, A6-48
model A7-23, B6-11, M9-1
functional B6-12
timing B6-13
register initialization A6-14, A6-48
register values A6-14, A6-30
ROMs M9-3
signals displayed A6-15, A6-30
timing A1-9, A7-23, B3-12, U4-4
trace format A6-13, A6-28
trace levels A6-14, A6-29, A6-49
unit-delay A1-9, A9-22
Xilinx ABEL simulator O14-10
single program enable
XC4000 Demonstration Board H2-12
size factor
report F3-10
slave mode U6-9, U6-14
slave serial mode U6-20
SLICE attribute
SLICE B4-103
SLICE module B4-2, B4-102
MAIN bus B4-102
SLICE B4-103
SUB B4-103
SUB bus B4-102
SUB_STARTS_AT B4-103
SLOW attribute O4-17, V4-7
SLOW property M4-8
SM# file A1-6, A1-8, A5-5, A5-6, A6-6, A6-35
sm_speed_opt option A6-41, A6-44
Snap menu V/ApC-25
snap-off command V/ApC-25
snap-on command V/ApC-25
soft macros L1-19, L1-20, L1-24, L1-25, L1-96, R1-111, V3-4, V3-7, V4-5, V11-77, V11-80, V11-81
description O11-45
software installation procedures, see Xilinx Installation Guide for details
software installation O2-2
solutions for tutorials (FPGA) O11-8
sourceless signals R2-42
SPC file
LCA2XNF R3-30
SPD file
APR R2-144
special function access symbols L1-7, L1-13, L1-31, L1-35, L1-40
speed command F2-40
accessing through XDM R1-34
speed grades R1-34, R3-15, R3-32, R3-33, R3-72, R3-185
speed option A1-9, A6-9, A6-25, A6-41, A9-5
speeds.xct file R2-128
split nets R3-30
splitting
variable specification E5-23
splitting equations E5-8
splitting outputs E5-18
spurs R3-186
SR flip-flops A1-11, A7-14
SRAM module B4-2, B4-106
BOUNDS B4-108
DEPTH B4-107
ENCODING B4-108
TNM B4-108
stack implementation V11-104, V11-105
STACK values V12-40
stand-alone-design option A6-11, A6-26
standard encoding A3-7, A6-9, A6-25, A6-38, A6-42, U3-5
standard option A1-10, A6-9, A6-25, A6-27, A6-39, A9-5

standard-listing option A6-12
starting XDM F2-2, F2-6, F/ApC-6
startup clock source (XC4000 only) R2-249
startup symbol V9-2
state diagrams A3-1
state expressions R1-2
state keyword A3-11, A4-1, A9-21, A9-27, V14-7
state machines V11-107, V11-109, V16-3
  converting encoded to symbolic A9-27
  design E1-3
  encoded A1-9, A3-5, A9-27
    example A3-13, A9-28
  encoding techniques A1-9, A3-4, A6-9, A6-25, A6-38, A6-42
    binary A3-6, A6-9, A6-25, A6-38, A6-42
    compromises A3-5
    one-hot A3-6, A6-9, A6-25, A6-35, A6-38, A6-42, A9-1, A9-5
    standard A3-7, A6-9, A6-25, A6-38
  entering design description A5-2, O4-21
  EPLD synthesis A5-6
  example A3-1
  FPGA synthesis A5-5
  implementations A3-4
  incompletely specified A1-11
  multiple A9-14
  optimizing A1-11
  options A6-9, A6-25
  parts A3-4
  speed-optimization option A1-11 , A6-10, A6-26
  state diagrams A3-1
  state tables A3-2
  symbolic A1-9, A3-5, A3-8, A9-22, A9-27, A9-31
  synthesis A5-2
    options A6-9, A6-25
state registers A3-4
state tables A3-1, A3-2, A3-3
state_diagram keyword A3-3, A3-12, A3-18, A9-21
state_diagram statement V14-9
state_register keyword A3-11, A4-1, A9-20, A9-21, A9-27
state_register statement V14-7
states
  clear U6-27
  configuration U6-34
  configuration cycle U6-28
  initialization U6-34
  memory clear U6-34
  power-up U6-34
  power-up and initialization U6-26
  reprogramming U6-31, U6-38
  start-up U6-29, U6-35
  XC2000 devices U6-25
  XC3000 devices U6-25
  XC4000 devices U6-32
state-splitting A6-10, A6-26
stateX
  error messages A6-6, A6-36, A/ApA-2
  purpose A1-6
static timing analysis R1-3, R1-5, U1-15, U4-5
  QueryNet U4-8
  XDelay U4-6
stay-in-current-state option A6-9, A6-25
stimulus and trace
  placing data on schematic O12-6
stimulus editor O12-19, O12-20, O12-21
stimulus file O12-16, O16-45
  editing STM file O16-50
  example file O12-16
STM file O12-17
  *see also* stimulus file
stop_on_miss option R2-197, R2-214, R2-219
stop-to-review-DRC option V13-20, V14-22
STRING statement F4-39

STYLE attribute B5-1
ACCUM B4-11
ADD_SUB B4-15
ANDBUS B4-3
COMPARE B4-34
COUNTER B4-40
DATA_REG B4-52
INC_DEC B4-66
selection B2-5
SHIFT B4-97
Usage B5-1
SUB attribute
SLICE B4-103
SUB_STARTS_AT attribute
SLICE B4-103
SUB-F-CI L1-105
SUB-FG-CI L1-105
SUB-G-1 L1-106
SUB-G-CI L1-107
SUB-G-F1 L1-106
SUB-G-F3- L1-107
subscripts option B/Ap-2
Sun R1-13
Sun 4 F2-4
supported software, displaying list of F2-37
SwapBlk command U9-20
switch matrices U1-12, U9-26
sym file V3-8
sym subdirectory V2-2, V3-8, V6-2, V8-2, V11-6, V11-9, V11-52, V12-29, V14-11
symatt option V/ApD-14
symattsize option V/ApD-14
symbol attributes O4-4
BLKNM O4-14
CAP O4-14
CMOS O4-14
DECODE O4-14
DEF O4-14
DOUBLE O4-14
FAST O4-14, O11-57
FILE O4-15
HBLKNM O4-15
HU_SET O4-15
INIT O4-15
LOC O4-15
MAP O4-15
MEDFAST O4-16
MEDSLOW O4-16
NODELAY O4-16
RES O4-16
RLOC O4-16
RLOC_ORIGIN O4-16
RLOC_RANGE O4-16
SLOW O4-17
table of O4-13
TNM O4-9, O4-17
TSidentifier O4-9, O4-17
TTL O4-17
U_SET O4-17
USE_RLOC O4-17
symbol locations R2-213, R2-219
symbol properties
see properties.
symbolic state machine A3-5, V14-7
symbols
ACLK V9-4, V11-89, V/ApE-20
adding pins M11-22
border V/ApD-9
BUF V11-142
BUFTs V4-3
BUS_DEF V13-7, V13-9
BUS_IF V4-16, V13-7
CLB V4-3, V/ApF-7
CLBMAP V4-3, V4-4, V15-10, V/ApE-1, V/ApE-2, V/ApF-7
conversion from XC3000 to XC4000 V/ApF-7
creating V11-31, V11-42, V16-47, V/ApA-3
creating for inclusion into schematic V3-9

symbols *(Continued)*
creating MemGen symbols O4-21
creating with SymGen A1-7, A5-9
creating Xilinx ABEL symbols O4-21, O14-11
CY4 V11-85
FMAP V4-3, V4-4, V11-85, V15-10
GCLK V11-89, V/ApE-20
generating top-level V/ApD-7
GXTL V9-4, V9-5, V/ApD-2, V/ApF-7
HMAP V4-3, V4-4, V15-10
IOB V4-3, V/ApF-7
latch V/ApD-11, V/ApD-16
MemGen V1-3
naming conventions V3-1, V3-3
OrCAD schematics O11-18
OSC V9-4, V9-5, V/ApD-2, V/ApE-4, V/ApF-7
OSC4 V/ApF-7
PAD V4-7, V5-3, V5-16
PLD V1-4, V5-4, V5-10, V5-13, V5-14, V5-15, V6-7, V7-10, V10-5, V10-13, V16-28
PULLUP V4-4, V4-5, V11-110
saving V11-41
sheet V5-17, V10-25
STARTUP V9-2
TIMEGRP V15-4, V15-6, V15-17
TIMESPEC V4-9, V15-4, V15-8, V15-17, V15-19
ViewGen V/ApD-14, V/ApD-15
WAND V4-4
X-BLOX V1-3, V4-16
Xilinx ABEL V1-3
symbols, custom E4-3
SymGen R1-19, V6-10, V14-11, V14-14, V14-15
accessing A5-10
EPLD designs A5-10
FPGA designs A5-10
input A5-9, A5-10
inputs A1-8
Mentor support A5-9
options A5-10
OrCAD support A5-9
output A5-9
program O4-21, O14-11
purpose A1-7, A5-9
Viewlogic support A5-9
sympinlth option V/ApD-14
sympinspc option V/ApD-15
SYN2XNF
accessing through XDM R1-22
SYNC_CTRL
ACCUM B4-10
CLK_DIV B4-29
COUNTER B4-38
DATA_REG B4-50
SHIFT B4-96
sync_reset keyword A3-12, A4-2
SYNC_VAL attribute B2-8
ACCUM B4-11
COUNTER B4-39
DATA_REG B4-50
SHIFT B4-97
usage B2-8
synchronous control B2-8
synchronous design U3-8
global clock distribution U3-8
synchronous reset L1-102
Synopsys U2-3
syntax conventions M10-2
syntax option A6-46
synthesis B6-4
synthesized logic R2-176
SynthX A4-18
compiling ABL file to XNF file A1-1, A5-5
error messages A/ApA-12
flip-flop mapping A1-11
incompletely-specified state machines A1-11

SynthX *(Continued)*
memory capacity A6-10, A6-26
number of CLBs used A6-9, A6-25
Obtaining help A6-43
optimizing state machines A1-11, A6-9, A6-25, A6-43
options
encode A6-42
errlog A6-42
family A6-43
help-all A6-43
mapped_xnf A6-43
old_library A6-43
optimize A6-43
output_directory A6-43
output_xnf A6-43
part-type A6-44
sm_speed_opt A6-44
unspecified_state A6-44
outputs A1-8
producing XNF file with primitives A6-43
purpose A1-6
report (REP) file A6-6, A6-35
running on command line A5-9, A6-42
selecting encoding method A6-42
selecting library version A6-43
selecting part family A6-43
setting behavior of incomplete state machines A6-44
specifying error log file name A6-42
specifying output file directory A6-43
specifying output file name A6-43
specifying part type A6-44
synthesizing state machines A6-9, A6-25
Synthx.log file A1-8, A5-11
System V Bourne Shell M10-1

## T

T flip-flops A1-11, A7-1
table option A6-49
table-format option A6-14
tabular option A6-28
tail bits U6-5
TAP U8-3, U8-7, U8-17
TAP controller U8-3, U8-4, U8-6, U8-10
TAP pins U8-3, U8-7
target device, choosing F2-17, F2-40
TBUF enable net R2-152
TBUF location
ANDBUS location attribute B4-4
TBUF output net R2-152
TBUFs R2-5, R2-10, R2-64, R2-126
I pin R3-19, R3-139
O pin R3-19, R3-139
T pin R3-19, R3-139
TCK L1-7, L1-13, L1-31, L1-35, L1-40, U8-3, U8-4, U8-6, U8-10, U8-14, U8-18
TDI L1-7, L1-13, L1-31, L1-35, L1-40, U8-3, U8-10, U8-14, U8-17
TDO U8-3, U8-4, U8-8, U8-9, U8-17
TDO pin pullup (XC4000 only) R2-248
TDO1 U8-10
TDO2 U8-10
Tektronix TEXHEX PROM format H4-2, R2-270, R2-271, R2-274, R2-278, R2-281
template file R3-17
XDelay R3-24
TERM_CNT
COUNTER B4-39
test access port *see* TAP
test clock *see* TCK
test data input *see* TDI
test data output *see* TDO
test mode select *see* TMS
test vectors A3-13, A3-19, A6-6, A6-11, A6-13, A6-14, A6-29, A6-45, A6-46, A9-25, V14-8, V14-9
test_vectors statement V14-9
text boxes A2-5

text editor
accessing from XDM O16-9, R1-30
my-text-editor-is command A5-3, A6-5
text editor, accessing from XDM F/ApC-10
text interface
in XDelay R3-23
Text menu V/ApC-16
text-based entry U1-15, U2-3
Verilog HDL U2-3
VHDL U2-3
Xilinx ABEL U2-3
Xilinx Synopsys Interface U2-3
text-create command V/ApC-16
text-delete command V/ApC-17
textsize option V/ApD-6
third-party design files
merging into OrCAD designs O4-21
adding symbol to schematic O4-22
creating a symbol O4-21
MemGen designs O4-21
Xilinx ABEL designs O4-21
three-state buffers L1-5, L1-46, V5-3
3-State multiplexing O5-7
three-state PLD outputs L1-15
three-state signals A7-10, A7-12
through-routes R2-183, R2-193, R2-195, R2-204, R2-211, R2-218, R2-220
tick size V/ApB-25
tick-size command V/ApB-25
time statement E2-3
TimeGroups
creating in XDelay R3-25
TIMEGRP attribute O4-8, R1-77
combining multiple groups R1-78
combining sets O15-6
flip-flops by output net name O15-8
grouping by exclusion R1-79
placement R1-78
syntax R1-77
text definitions O15-26
TIMEGRP constraints L1-54
TIMEGRP primitive R1-77
TIMEGRP statements R2-36, R2-37
TIMEGRP symbol V15-4
clock edges V15-7
combining sets V15-7, V15-17
defining sets by output net names V15-7, V15-8
EXCEPT statement V15-7, V15-9
purpose V15-6
TIMESPEC attribute O4-7, O15-9
text specifications O15-26
TIMESPEC constraints L1-52
TIMESPEC primitives M4-12, R1-70
TIMESPEC statements R2-36, R2-37
TIMESPEC symbol A1-10, V15-4
placing on schematic V15-11
purpose V15-8
specifying timing constraints V15-19
TNM attribute V15-17
TSidentifier attribute V4-9
timing analysis R3-15
timing analysis, *see* XDelay O15-34
timing attributes, *see* XACT-Performance
timing calculations
clock-to-output E5-9, E5-13, E5-19
example E5-9, E5-12
for equation splitting E5-18
maximum frequency E5-10, E5-14
output enab./disab. E5-10
propagation delay E5-10
setup and hold E5-9, E5-13
timing margins R3-27
Timing menu R3-3
timing option R2-192, R2-215, R2-218
timing requirements R1-4, R1-69
timing simulation A1-9, A7-23, B3-12, M1-2, M8-1, O8-1, U4-4
auto generate M8-3
back-annotation B3-12
command file V12-52
creating VST and DBA files O10-16

timing simulation *(Continued)*
design flow V8-2, V8-3, V8-4
EPLD manual translation V10-16
FPGA manual translation V10-13, V10-14, V12-2
XSimMake V1-4, V12-2
designs with MemGen components V8-2, V12-49
designs with special symbols V8-2
designs with X-BLOX modules V8-2, V13-21, V13-23
designs with Xilinx ABEL components V8-2, V12-49, V14-24, V14-26
designs without special symbols V8-2
EPLD designs O16-42
creating VST and DBA files O10-17
input vectors O16-43
XSimMake summary O8-5
EPLD net visibility V9-7
EPLDs V1-4, V8-2, V8-3, V8-5, V10-16, V16-37, V16-39
FPGA designs
creating VST and DBA files O10-16, O12-28
summary O12-26
XSimMake summary O8-5
generating netlist manually V10-13
generating netlist with XSimMake V1-4, V8-1, V12-1, V12-48, V12-49, V16-37
input V8-2
LCA2XNF R3-29
manual translation M10-14
output V8-2, V12-50
output files M8-4
performing functional simulation first V6-3, V8-1, V8-3, V12-29
purpose V8-1
see also PLD_TIMSIM8, TIMSIM8
simulating in ViewSim V12-52, V16-41
use original M8-3
viewing back-annotated values V16-44
viewing waveforms in ViewWave V12-52, V16-43
timing specification R1-69, U2-5
timing specification properties
adding TIMESPEC/TIMEGRP M4-11
adding TS flag M4-12
see also properties
TS Flag M4-11
timing *see* XACT-performance O15-6
timing-flagblk command V15-30
timing-query-template command V15-31
timsim8 M8-1
manual translation M10-1
options M10-28
syntax M10-27
variables M10-28
timsim8.log M8-4
timsim8.sh M8-4
title keyword V16-29
title statement A3-10, A3-16, A9-20, A9-24, E2-2, V14-6
TMS L1-7, L1-13, L1-31, L1-35, L1-40, U8-3, U8-4, U8-10, U8-14
TMV file A1-6, A1-8, A5-3, A6-11, A6-13, A6-14, A6-16, A6-29, A6-31, A6-33, A6-34, A6-46
TNM attribute B2-31, O4-9, O4-17, O15-4, O15-11
ACCUM B4-12
adding to schematic V15-11
architectures L1-42
BIDIR_IO B4-21
CLK_DIV B4-30
COUNTER B4-42
DATA_REG B4-52
defining sets V15-14
forward tracing V15-5
grouping symbols by predefined sets V15-6
INPUTS B4-70

TNM attribute *(Continued)*
macros V15-5, V15-17
nets V15-5
OUTPUTS B4-82
primitives V15-4, V15-17
PROM B4-86
purpose L1-42, V4-9, V15-4
SHIFT B4-99
SRAM B4-108
syntax L1-43, V15-5
TRISTATE B4-111
TNM property M4-11
TNMs R1-73
grouping flip–flops R1-76
incompatible symbols R1-74
on clock pins R1-77
on macro symbols R1-74
on primitive symbols R1-73
on signal R1-76
placement on schematic R1-73
To option V15-43
ToAll option V15-43
ToFF option V15-29, V15-41
toggle flip-flops A4-14, A7-14
ToIOB option V15-43
toolbar icons A2-5
top-level file E1-1, E2-1, R2-1
editing E3-10
trace command V12-45
trace data O12-6
trace file
example file O12-17
trace option A6-48
trace simulation levels A6-14, A6-49
trace-format option A6-28
trace-simulation levels A6-29
trace-type option A6-29
translate ABL2PLD command A5-8
translate ABL2XNF command A5-7
translate HM2RPM command R1-117
Translate menu F2-18, L1-21, R1-19, V5-13, V5-16, V7-4, V7-8, V7-13, V7-14, V10-2, V11-118, V11-145
command E4-4, E4-7
translate-XEMAKE command V16-37
translate-XMAKE command V14-22
translate-JED2PLD command V16-34
translate-pinsave command A7-17, A7-18, A7-19, A7-21, V16-34, V16-36
translate-PLUSASM command A7-19, V16-33, V16-35
translate-WIR2XNF command V16-33
translate-XEMAKE command V7-8, V16-33
translate-XMAKE command V13-18, V15-23
translate-XNFMERGE command V16-33
translation
*see also* retarget design
Calc design O11-74
creating a timing netlist file O10-16
EPLD designs
automatic implementation O7-7
FPGA designs
automatic implementation O7-2
commands O11-102
functional netlist creation O6-1
timing netlist creation O8-1
FPGA Incremental designs
commands O11-103
incremental designs O11-99
manual translation O10-2
RPMs O1-4
SDT2XNF O1-3
stimulus and trace files O12-17
XNF2VST O1-3
XSimMake O6-1
translator see integrator
TRC file O12-17
*see also* trace file
TREE structure comparisons B4-34
TREE style B4-34
TRIG U7-7

tri-state, see also 3-State F4-65
tri-state
  3-State M9-3
  control equation (TRST) F4-65
  control E2-11, E3-17, E3-18
  outputs E2-17
TRISTATE module B4-2, B4-110
  FLOAT_VAL B4-111
  LOC B4-111
  TNM B4-111
TRST equation F4-65
TS attribute R1-70, V4-9
  basic path types R1-86
  c2p R1-89
  c2s R1-86
  delay R1-83, R1-94
  delay time units R1-82
  length R1-70
  p2p R1-90
  p2s R1-88
  placement R1-72
  specifying in terms of another R1-83
TS flags M4-11, M4-12, R1-86, R1-94
  attached to clock net R1-96
  c2p paths R1-96
  default specifications R1-95
  non–default specifications R1-95
  on cascaded counters R1-99
  p2s path R1-97
  placement on schematic R1-95
TS identifier attribute B2-31, O4-9, O4-17, V4-9
  architectures L1-43
  purpose L1-43
  syntax L1-43
TS identifier property M4-11
TSMaxpaths option V15-28, V15-34
TT1 file A1-6, A1-8
TT2 file A1-6, A1-8
TTL attribute O4-17, V4-8
  architectures L1-44
  purpose L1-44
  syntax L1-44
TTL property M4-9
tutorial
  design entry (SDT) O11-1
  design files O11-8
  directory F5-13
  example design F/ApC-2
  example files F/ApC-4
  simulation (VST) O12-1
  XACT-performance O15-1
  X-BLOX O13-1
  XDelay O15-1
  XEPLD command summary O/ApD-1
  Xilinx ABEL O14-1
tutorial directory F/ApC-9, F/ApC-10
TWO_COMP encoding B2-17
TXT files F5-13
tying the design U6-2
type command V11-120

## U

U_SET attribute O4-17
U_SET constraint L1-87, L1-94, V4-6
  architectures L1-45
  purpose L1-45, L1-75
  syntax L1-46, L1-75
  use with USE_RLOC constraint L1-92
U_SET property M4-7
UART
  example design F/ApC-2
UART_EQN.PLD file F/ApC-17, F/ApC-18
UIM E2-4
  AND functions E2-13, E5-5, E5-12
  and interconnector integrator module F5-9
  interconnections E2-13
  optimization E5-13
  using E2-13
UIM feedback E3-15, E3-17

UIM optimization L1-44
UIM_OPT attribute O5-21, V5-18
  architectures L1-44
  purpose L1-44
  syntax L1-45
UIM_OPT property M5-16, M5-20
UNAKAXNF M10-15, M10-17
  error messages M/Ap-7
  options M10-28
  syntax M10-28
unconnected pins R1-111
undo command V16-1, V/ApA-35
Undo menu V/ApA-35
undo-off command V/ApA-40
undo-on command V/ApA-40
unguided signals R2-182
unified libraries L1-72, V1-3, V11-14
  retargeting design M2-6
unified libraries A6-10, A6-26, A6-40, A6-43, M1-8, M3-4, O4-2, R1-111, R1-112, R1-113, R1-114, R1-116, R1-117, R1-119, V3-4, V3-5, V6-6, V7-5, V11-31, V11-69, V12-29, V12-49, V/ApF-1
  description O1-3
  format O1-4
  names O1-3
unit-delay simulation A1-9, A9-22, V12-42, V12-48
universal asynchronous receiver transmitter V16-2
universal counter B4-36
universal interconnect matrix (UIM) A7-1, L1-7, V5-6, V5-18, V5-19, V5-20, V9-7
universal shift register B4-92
UNIX V12-8, V16-5
unknown simulation values O9-1
unspecified_state option A6-9, A6-25, A6-41, A6-44
unused resources, munching F5-3
UP_DN
  COUNTER B4-37
UPAD L1-5, L1-7, L1-13, L1-20, V5-16
use .tmv file option A6-14, A6-29
use_faster_c2s option R2-196, R2-215, R2-219
USE_RLOC attribute B5-3, O4-17
  ACCUM B4-12
  ADD_SUB B4-16
  COUNTER B4-41
  DATA_REG B4-51
  INC_DEC B4-66
  SHIFT B4-98
USE_RLOC constraint V4-6
  architectures L1-45
  purpose L1-45, L1-90
  syntax L1-45, L1-90
  using with U_SET L1-92
USE_RLOC property M4-7
use-all-available-memory option A6-10, A6-26
UseCriticalNetsLast U6-2
use-old-library option A6-10, A6-26
user attribute O4-6
user registers U8-10
  connections U8-10
user_search_path option R2-216
User1 U8-10, U8-15, U8-17
User2 U8-10, U8-15, U8-17
user-created libraries O3-7, V2-12, V3-7
user-created symbols L1-19
user-defined option A6-32
Utilities menu F2-17, F2-33, R1-19, R1-29, V11-119, V12-31, V12-50
  command E3-9
utilities-browse command V16-29, V16-35
utilities-directory command V16-1, V16-9, V16-10
utilities-DOS command V11-119, V11-139, V12-31, V12-50
utilities-edit command V16-29, V16-35
utilities-scandisk command V11-16

## V

VALUE attribute
  FORCE B4-63
value-on command V/ApC-13
Values menu V/ApC-13
values-anno-off command V/ApC-13
values-anno-on command V/ApC-13
values-off command V/ApC-13
variables
  editor F/ApC-5
  XACT F/ApC-5
VCC O10-11, V3-2, V5-13, V11-110, V11-141, V11-142
VCC symbol O4-20
  EPLD M5-15
  EPLD designs O5-14
vector command V12-39
vector option A6-46
vectorized labels V/ApA-11
vectors V14-7, V/ApB-2, V/ApB-3, V/ApB-4, V/ApB-5, V/ApB-6, V/ApB-7, V/ApB-8, V/ApB-9, V/ApB-10, V/ApB-13, V/ApB-14, V/ApB-16, V/ApB-22
verbose U6-2
verification E5-5
  design fit E5-5
  design timing E5-8
  XChecker O11-86
Verify menu E5-4, F2-28, R1-26, R2-273, V8-4, V10-2, V10-19, V10-21, V10-22, V11-135, V12-30, V12-49, V15-30, V16-37
verifying 3V Adapter operation
  XChecker H5-12
verify-makejed command A7-21, V16-37
verify-makeprg command A7-18, A7-19, V16-37
verify-vmh2xnf command A7-23, V10-22, V16-38
verify-vsm command A7-23, V10-19, V16-38
verify-vsmupd command V10-21
verify-xnf2vst command A7-23
verify-xnf2wir command A7-23, V16-38
verify-xsimmake command V6-5, V12-30, V12-49, V13-12, V13-21, V14-17, V14-24, V16-37
Verilog HDL U2-3
version command F2-37
  accessing through XDM R1-32
VHDL L1-1, V1-2
VHSIC HDL (VHDL) U2-3
View menu A6-5
  ViewDraw V/ApA-4
  ViewWave V/ApC-2
ViewBase V/ApE-4, V/ApE-22
view-compiled-equations command A5-7, A6-6
view-compiler-listing command A5-7, A6-5
ViewDraw
  adding boxes to schematic V11-32, V/ApA-13
  adding bus labels to schematic V11-62, V11-71, V16-24, V/ApA-10
  adding buses to schematic V11-58, V11-71, V16-19, V/ApA-12
  adding component labels to schematic V11-73
  adding components to schematic V11-45, V16-16, V16-49, V/ApA-8
  adding labels to symbol pins V11-34
  adding net attributes V11-97
  adding net labels to schematic V11-60, V11-71, V16-22, V/ApA-10
  adding nets to schematic V11-52, V11-71, V16-20, V16-21, V/ApA-7
  adding overscores to labels V3-2
  adding pins to schematic V11-33, V/ApA-13
  adding text to schematic V11-39, V/ApA-14

ViewDraw *(Continued)*
adding X-BLOX elements to schematic V13-6
adding X-BLOX module V13-3
assigning pin locations V11-95
assigning signals to XEPLD pins V16-27
attributes V3-6, V11-36, V11-94, V11-96, V11-99, V16-25, V/ApA-11, V/ApA-21, V/ApA-22, V/ApA-36
attributes *see also* attributes
bus names V3-3
changing components on schematic V11-66, V/ApA-26
changing label sense V/ApA-21
changing pin sense V/ApA-23
changing sheet size V11-32, V16-15, V/ApA-20
changing text V/ApA-25
changing text size V11-38, V/ApA-24
checking schematic V11-112
closing all windows V/ApA-4
closing schematic window V11-30, V/ApA-3
component names V3-3
configuring environment V2-1
configuring viewdraw.ini file *see also* viewdraw.ini file V2-4
connecting components with nets V11-54
connecting nets to pins on schematic V11-56
context window V11-28, V16-15, V/ApA-23
copying schematic V11-65
copying schematic components V11-49, V/ApA-33
creating arrays V/ApA-25
creating schematic V11-26, V11-44, V16-11, V16-15
creating symbols V3-9, V11-31, V11-42, V/ApA-3
creating VSM file V12-9, V/ApA-26
creating WIR file V/ApA-27
deleting nets V11-57
deleting objects V16-17, V/ApA-32
deselecting objects V/ApA-31
design flow V1-4, V11-1
displaying dialog box V/ApA-39
environments V1-1
examining back-annotated values V9-8
exiting V/ApA-38
finishing schematic V11-67, V16-26
function keys *see* function keys
generating WIR file V11-112
grid V/ApA-24
help V/ApA-36
help screen V2-15, V11-19
including third-party designs V3-9
installing tutorial software V11-4, V11-5, V11-12
invoking V2-12
keyboard commands V2-14, V11-20, V11-21, V/ApA-39
library aliases *see* library aliases
listing component labels V/ApA-37
listing object descriptions V14-15, V/ApA-37
listing schematics V/ApA-18
listing schematics and symbols V/ApA-17, V/ApA-18
menu commands V11-19, V11-21, V/ApA-1
menu structure V2-15
menus
Add V/ApA-7
Bye V/ApA-38
Change V/ApA-20
Copy V/ApA-33
Delete V/ApA-32
Export V/ApA-26
File V/ApA-16

ViewDraw, menus *(Continued)*
Info V/ApA-36
Level V/ApA-14
Move V/ApA-33
Plot V/ApA-35
Select V/ApA-29
Undo V/ApA-35
View V/ApA-4
Window V/ApA-2
Xform V/ApA-27
mirroring objects V/ApA-28
mouse operation V2-14, V11-17
moving objects V11-50, V16-17, V/ApA-33
multiple-sheet designs V3-1
naming conventions V3-1
opening schematic window V11-26, V11-88, V12-6, V12-33, V12-52, V14-12, V16-12, V/ApA-2
panning V11-30, V/ApA-5
placing custom components V11-68
plotting schematics V/ApA-35
popping back to previous level of hierarchy V/ApA-15
purpose V1-2
pushing into schematic or symbol sheet sets V/ApA-15
pushing into underlying schematic V11-76, V/ApA-14
pushing into underlying symbol block V/ApA-15
reading file V/ApA-17
refreshing window V/ApA-4
renaming schematics in DOS V16-28
replacing block with Xilinx ABEL module V14-12
reserved names V3-2
restoring files V/ApA-19
rotating objects V16-17, V/ApA-27
saving log file V/ApA-19
saving schematic V11-51, V11-76, V11-103, V16-28, V/ApA-16, V/ApA-40
saving symbol V11-41, V/ApA-16
scaling objects V/ApA-28
scrolling window V/ApA-6
selecting attributes V/ApA-30
selecting components V/ApA-31
selecting components and labels V/ApA-30
selecting groups of objects V/ApA-32
selecting labels V/ApA-29
stretching objects V/ApA-29
terminating dangling nets V16-22, V/ApA-39
turning off attribute visibility V11-39, V/ApA-22
turning off label visibility V/ApA-20
undoing commands V/ApA-35, V/ApA-40
using XC3000 designs as basis for XC4000 V/ApF-7
verifying Xilinx ABEL symbol attributes V14-15
verifying Xilinx ABEL symbol type V14-14
viewing oscillator schematic V11-88
viewing relationally placed macros V11-83
viewing schematic V11-27, V12-51, V14-14, V16-16, V/ApA-6
viewing selected objects V/ApA-7
viewing soft macro schematics V11-77
viewing soft macro symbols V11-81
viewing stack implementation V11-104
viewing state machines V11-107
viewing Xilinx library primitives V11-80
X-BLOX buses V4-16, V13-6, V13-7, V13-9
zooming V11-30, V16-15, V/ApA-5, V/ApA-6

Viewdraw macro file
MemGen R1-60
viewdraw.ini file
adding library V2-6, V2-7, V3-8
adistance option V/ApD-6, V/ApD-10, V/ApD-12
builtin library V2-5, V2-7, V2-12, V3-8, V11-9, V11-14, V11-80
changing library aliases V3-5, V/ApF-1
changing library aliases *see also* Altran V11-13
configuring V2-4, V12-5, V13-2, V13-3, V14-2, V14-3, V15-2, V15-4, V16-12
dialog-box option V/ApA-2, V/ApA-8, V/ApA-26, V/ApA-31
DIR keyword V2-4, V2-6, V11-8, V11-14, V/ApD-6, V/ApF-1, V/ApF-2, V/ApF-3, V/ApF-5, V/ApF-6
editing by XSimMake V6-2, V8-2, V12-29
editing with text editor V2-6, V11-7, V11-9, V11-45
editing with ViewFile V2-7, V16-12
GRID option V/ApD-6
insertion of simulation directory V13-12, V14-17
library aliases V2-5, V2-8, V2-11, V3-8, V11-8, V11-45, V/ApF-5
listing all schematics in ViewDraw directories V/ApA-18
listing all symbol files in ViewDraw directories V/ApA-18
netname option V10-24, V/ApD-6
placement in directory V10-19, V11-9
purpose V11-7, V13-3, V14-3, V15-3
route option V/ApA-8, V/ApA-12
search order V2-5, V2-8, V10-25, V11-9, V16-12, V16-47
sheet size V/ApA-20
SHM4000 library V2-6, V2-12, V6-8
syntax V2-4, V2-6, V2-7, V11-8, V11-14
template V11-7
textsize option V/ApD-6
user-created libraries V2-12, V3-8
X-BLOX library V4-16, V11-8, V13-3
view-errors command A5-3, A5-6, A6-6
ViewFault V/ApD-4
ViewFile
creating project directory V2-3, V11-9, V11-23, V11-25, V16-12
exiting V2-4, V11-25, V16-12
modifying directory search order in viewdraw.ini file V2-7, V16-12, V16-47
opening V2-3, V16-12, V16-47
purpose V2-3
view-file command A6-6
view-full command
ViewDraw V16-16, V16-27, V/ApA-4, V/ApA-6
ViewWave V/ApC-4
ViewGen V10-17
adding component labels V/ApD-15
attribute visibility V10-24
command file V/ApD-5
connectivity V10-24
controlling level assignment V/ApD-12
deleting nets V/ApD-15
environments V1-1
error messages V/ApE-14
flattening design V/ApD-10
generating top-level symbol V/ApD-7
help V/ApD-7
help on advanced options V/ApD-11
identifying symbols for -latchbflevel V/ApD-16
inputs V10-23
invoking V10-25
label visibility V10-24

ViewGen *(Continued)*
limiting number of logic levels V/ApD-11
multiple WIR files V10-28
options
-analyze V/ApD-15
-attr V10-26, V10-27
-busmane V/ApD-9
-c V/ApD-6, V/ApD-7, V/ApE-15
-compcomp V/ApD-10
-complabels V/ApD-15
-compnet V/ApD-10
-comptext V/ApD-10
-deletenet V/ApD-15
-flatten V/ApD-10
-gridsize V/ApD-10
-heightlimit V/ApD-11, V/ApE-18, V/ApE-19
-help V/ApD-7
-helpadv V/ApD-11
-i V/ApD-7
-inpin V/ApD-11
-labelpos V/ApD-15
-latchfblevel V/ApD-11
-latchsym V/ApD-16
-levellimit V/ApD-11, V/ApE-18
-loadlevel V/ApD-12
-makesym V/ApD-7
-maxsheet V/ApD-16, V/ApE-16
-minsheet V/ApD-16, V/ApE-16
-noschem V/ApD-7
-o V/ApD-8
-outfblevel V/ApD-12
-outpin V/ApD-13
-permute V/ApD-13, V/ApE-16, V/ApE-17, V/ApE-18, V/ApE-20
-permuteinputs V/ApD-13
-pinlblsize V/ApD-14
-quiet V/ApD-8
-restart V/ApD-8, V/ApD-14, V/ApE-18
-Sheet V/ApD-6
-sheet V/ApD-8, V/ApD-9, V/ApE-16
-Sheetsym V10-26, V/ApE-15
-symatt V/ApD-14
-symattsize V/ApD-14
-sympinlth V/ApD-14
-sympinspc V/ApD-15
-timeformat V10-27
-visattr V/ApD-17
outputs V10-25
printing netlist errors V/ApD-15
purpose V1-2, V10-1, V10-23
requirements V10-23
schematic format V10-24
setting component spacing V/ApD-10
setting grid size V/ApD-10
setting minimum net spacing V/ApD-12
setting net/component spacing V/ApD-10
setting text label/component spacing V/ApD-10
sheet symbols V10-25
specifying
attribute text size V/ApD-14
border symbol name V/ApD-9
bus name V/ApD-9
command file V/ApD-7
default labels V/ApD-15
I/O pin names V/ApD-11
input file in command file V/ApD-7
logic level limit V/ApD-11
maximum column height V/ApD-11
maximum sheet size V/ApD-16
minimum sheet size V/ApD-16
netlist flattening level V/ApD-12
non-standard sheet size V/ApD-9

ViewGen, specifying *(Continued)*
output file in command file V/ApD-7
output pin name V/ApD-12
permutable inputs V/ApD-13
pin label size V/ApD-14
pin spacing V/ApD-15
restart times V/ApD-14
sheet size V/ApD-8
symbol length V/ApD-14
symbols with permutable inputs V/ApD-13
top-level symbol attributes V/ApD-14
visible attributes V/ApD-17
suppressing message display V/ApD-8
suppressing schematic generation V/ApD-7
viewgen.cmd file V/ApD-5
viewgen.ini file V/ApD-6, V/ApD-9
VIEWGENOPT environment variable V/ApD-6
view-in command
ViewDraw V11-30, V16-16, V/ApA-5
ViewWave V/ApC-4
viewing files F2-34, F2-35
Viewlogic A1-5, A7-23, R1-38
input to XMake R1-38
Viewlogic Viewdraw A1-7, A5-9
Viewlogic Viewdraw symbol R1-65
ViewLogic Viewsim E5-4
Viewlogic Viewwave H5-40
Viewlogic_Epld_Timing command V8-4, V16-38
Viewlogic_Fpga_Func command V6-5, V12-31, V13-12, V14-17
Viewlogic_Fpga_Timing command V8-4, V12-49, V13-21, V14-24
view-out command
ViewDraw V11-30, V16-16, V/ApA-6
ViewWave V/ApC-4
view-pan command
ViewDraw V11-30, V/ApA-5
ViewWave V/ApC-3
viewpoint M6-5
back-annotation M6-9, M10-26
default M10-26
functional simulation M6-4
simulation M6-9, M10-7
timing simulation M8-3
XNF M6-9, M10-25
view-range command V/ApC-5
view-refresh command
ViewDraw V11-39, V/ApA-4
ViewWave V/ApC-2
view-scroll command V11-30, V/ApA-6
ViewSim V11-80
asserting global reset V12-17
assigning bit patterns V/ApB-14
assigning values to clock V12-16
assigning waveform values V/ApB-3, V/ApB-6
back-annotation *see* back-annotation
changing tick size V/ApB-25
checking setup and hold time V9-3
closing window V9-8
command file V9-7, V9-8, V9-9, V11-10, V12-28, V12-35, V12-39, V12-44, V12-45, V12-52, V13-18, V16-40, V/ApB-20, V/ApC-7, V/ApC-11, V/ApC-17
creating waveform view V9-8
creating Workview project directory V12-5
decrementing waveform values V/ApB-3
defining input node/vector patterns V/ApB-6
defining vectors V12-16, V/ApB-2
displaying changed nodes V/ApB-12
displaying critical path V/ApB-13

ViewSim *(Continued)*
displaying information V/ApB-14
displaying input nodes V/ApB-12
displaying RAM/ROM contents V/ApB-23
displaying status V/ApB-13
environments V1-1
examining simulation values on schematic V12-22, V12-56
functional simulation V6-10, V12-5, V13-18, V14-20
halting V/ApB-8
hyphen V3-1
including builtin library V2-7, V2-12
incrementing waveform values V/ApB-4
initializing flip-flops V9-1
keyboard commands V/ApB-21
loading RAM/ROM addresses V/ApB-24
log file V9-8
memory requirements V/ApD-3
menus
Assign V/ApB-14
Cycle V/ApB-20
Display V/ApB-12
Execute V/ApB-20
Force V/ApB-16
Release V/ApB-18
Run V/ApB-18
Setup V/ApB-1
Sim V/ApB-19
multiplying waveform values V/ApB-5
opening log file V/ApB-11
opening ViewWave window V12-14
opening window V9-7, V12-12, V12-35, V13-23, V14-20, V14-26, V16-41
printing trace changes V/ApB-10
purpose V1-2, V12-1
repeating commands at intervals V/ApB-23
resetting nodes to high impedance V/ApB-18
running V/ApB-18
saving node values V/ApB-24
saving waveforms in file V9-9
selecting nets for simulation V12-10
setting
breakpoint V/ApB-8
defaults V/ApB-11
execution start time V/ApB-21
nodes/vector High V/ApB-16
nodes/vector Low V/ApB-16
nodes/vectors unknown V/ApB-17
number of cycles V/ApB-20
simulation time V/ApB-19
ViewWave stream V12-13, V/ApB-2
simulating
circuit V12-19
EPLD DESIGNS V16-41
EPLD designs V9-5, V16-54
GXTL symbol V9-5
OSC oscillator V9-4
flow V12-2
simulator E5-3
specifying clock transitions V/ApB-7
specifying radix V/ApB-8
specifying step duration V/ApB-7
specifying watch list V/ApB-10
timing simulation V8-2, V12-52, V13-23, V14-26, V16-41
tutorial files V12-4
verifying node/vector values V/ApB-22
wirelist file F2-30, F2-31, F2-32
viewsim.log file V9-8, V12-35, V12-36, V/ApB-21
view-simulation-results command A5-5, A5-6, A6-6, A9-26, A9-37

ViewSynthesis
architectures supported V1-2
environments V1-1
purpose V1-2
ViewText V12-35, V12-45
view-view-file command A5-7
ViewWave V14-21, V16-40, V16-41, V16-43
adding signals from ViewDraw schematic V/ApC-6
adding text V/ApC-16
adding waveforms V/ApC-5, V/ApC-7
adding waveforms to buffer V/ApC-11
back-annotating simulation values *see* back-annotation
changing grid display space V/ApC-25
changing waveform color V/ApC-26
closing window V12-43
command file V/ApC-11
controlling grid-snapping V/ApC-25
copying waveforms V/ApC-8
copying waveforms to buffer V/ApC-9, V/ApC-20
creating buses V/ApC-16
creating waveform view V9-8
deleting text V/ApC-17
disabling edit mode V/ApC-19
displaying grid V/ApC-24
displaying timeline V/ApC-24
displaying waveform list V/ApC-26
displaying waveform values V/ApC-13
dividing bus V/ApC-16
editing waveforms V/ApC-18
environments V1-1
grid V/ApC-24
help V/ApC-26
inserting waveform values V/ApC-17
inverting logic values V/ApC-15
measuring time V12-41
menus
Buffer V/ApC-9
Color V/ApC-26
Display V/ApC-24
Edit V/ApC-17
File V/ApC-11
Grid V/ApC-24
Info V/ApC-26
Modify V/ApC-15
Radix V/ApC-14
Signals V/ApC-5
Snap V/ApC-25
Text V/ApC-16
Value V/ApC-13
View V/ApC-2
Window V/ApC-1
opening window V12-14, V12-39, V12-52, V13-18, V13-23, V16-43, V/ApC-2
panning V/ApC-3
pasting waveforms from buffer V/ApC-10, V/ApC-21
purpose V1-2, V12-1
reading saved file V/ApC-12
refreshing window V/ApC-2
removing waveforms V/ApC-6, V/ApC-7
removing waveforms to buffer V/ApC-10, V/ApC-20
renaming waveforms V/ApC-8
repeating waveforms V/ApC-19
saving waveforms in file V9-9, V12-28, V/ApC-1, V/ApC-12
scrolling V/ApC-9
selecting all waveforms V/ApC-9
setting binary radix V/ApC-14
setting decimal radix V/ApC-14
setting hexadecimal radix V/ApC-15
setting octal radix V/ApC-14
specifying time range V/ApC-22

ViewWave *(Continued)*
specifying time units V/ApC-22
transferring data from ViewSim V12-13, V/ApB-2
verifying timing V12-54
viewing full simulation V/ApC-4
viewing simulation range V/ApC-5
viewing waveforms V9-8
zooming V12-26, V/ApC-3, V/ApC-4
view-Xilinx-EPLD-equations command A5-7, A6-6
view-Xilinx-SYNTHX-report command A5-6, A6-6
view-zoom command
ViewDraw V11-30, V16-16, V/ApA-5
ViewWave V/ApC-3
visattr option V/ApD-17
visible option M8-5
VMD file E5-4, F5-15, M7-7, V10-16, V10-22
VMF file A7-21, F2-18, F2-23, F/ApC-20, F/ApC-22, L1-21, O16-40, V5-16, V16-34
VMH file E5-4, F5-15, M7-6, M7-7, O7-1, O7-12, O16-37, V1-4, V7-1, V7-7, V7-8, V7-10, V7-12, V7-13, V8-1, V10-16, V10-22, V16-34
VMH/VMD file M5-14, M8-1, M8-3
VMH/VMD files M3-9, M7-1
VMH2VST A7-18, A7-19, A7-20
VMH2VST command
example F/ApC-23
VMH2WIR command F2-32
example F/ApC-23
VMH2XNF M10-18, V10-17
accessing through XDM R1-27
changing output file name V/ApD-5
choosing library version V/ApD-5
generating timing simulation netlist manually V10-16
generating timing simulation netlist with XSimMake V8-3, V16-38
inputs V10-22
invoking V10-16
menu command E5-4
command line V10-22
XDM V10-22
options
-l4 V/ApD-5
-l5 V/ApD-5
-o V/ApD-5
outputs V10-23
program description M10-29, O10-18
purpose V10-22
voltage regulator
XC4000 Demonstration Board H2-5
vsimtemp.log file V9-8, V12-35, V12-36
VSM A7-18, A7-19, A7-20, V10-17
accessing through XDM R1-27
command F2-30
examlpe F/ApC-23
design flow V1-4
error messages V/ApE-12
generating design with flattened connectivity V/ApD-4
generating hierarchical net name equivalents V/ApD-3
generating simulation netlist V6-1, V10-5, V10-9, V10-10, V10-12, V10-15, V10-17, V10-19
including fault simulation records V/ApD-4
inputs V10-20
invoking
command line V10-9, V10-10, V10-12, V10-15, V10-17, V10-19
XDM V10-19
options
-d V/ApD-3
-f V/ApD-3
-h V/ApD-3
-s V/ApD-3
-t V/ApD-4
-w V/ApD-4

VSM *(Continued)*
outputs V10-20
purpose V10-9, V10-10, V10-19
referencing nets by top-level names V/ApD-3
running with XSimMake V8-4, V13-16, V14-20, V16-38
specifying back-annotation table file name V/ApD-3
specifying output VSM file name V/ApD-3
warning messages V/ApE-10
VSM file V1-4, V6-2, V6-3, V6-7, V6-9, V6-10, V8-2, V10-5, V10-8, V10-9, V10-10, V10-12, V10-15, V10-20, V10-22, V12-9, V12-49, V12-58, V13-23, V14-25, V14-26, V16-38, V16-54, V/ApE-13
VSM netlist A1-12
VSMUPD V10-17
accessing through XDM R1-27
adding net equivalences V10-10, V10-12
creating specified VSM file V/ApD-4
error messages V/ApE-13
generating simulation netlist V10-5, V10-9, V10-20, V13-23, V14-26
inputs V10-20, V10-21
invoking
command line V10-10, V10-21
XDM V10-21
options
-b V/ApD-4
-o V10-22, V/ApD-4, V/ApE-13
-x V10-22, V/ApD-4
outputs V10-22
purpose V10-20
specifying XNF file name V/ApD-4
suppressing output messages V/ApD-4
warning messages V/ApE-13
VST
software installation O2-2
VST file E5-3, F2-29, F/ApC-23, O10-16, O10-20
vst.cfg file O12-3
sample file O2-12
VST386+ O6-1
configuration O12-4

## W

W attribute V3-7
W net attribute L1-34, V4-10
WAND L1-19, L1-20, L1-54, L1-69, L1-70
WAND symbols V4-4
WAND1 L1-11
warning messages R1-58
SDT2XNF O/ApC-2
XDraft O/ApC-1
XNF2VST O/ApC-4
warnings F5-16
watch command V12-44
watch list V/ApB-19
wave command V9-8, V9-9, V12-39
wave option A6-49
wave-format option A6-13
wave-format-ASCII option A6-13
waveforms A6-13, V9-9, V12-15, V12-20, V12-27, V12-35, V12-39, V12-52, V12-53, V/ApB-3, V/ApB-4, V/ApB-5, V/ApB-6, V/ApB-18, V/ApC-5, V/ApC-6, V/ApC-7, V/ApC-9
wdir directory V/ApD-6
wdir environment variable V11-16, V12-6, V16-5, V/ApD-6, V/ApE-12
weight constraints L1-52
weight flag O4-19
weight-net constraint R2-153
weight-net attribute *see* W net attribute
WFM file V/ApC-1, V/ApC-13
when_routable setting R2-215
whole_sigs setting
guide_routing option R2-203

guide_thru_routes option R2-178, R2-183, R2-204
lock_routing option R2-178, R2-183, R2-207
wide-edge decoders L1-11, L1-20, V11-104, V11-109, V11-111
ANDBUS DECODE style B4-3
wildcards L1-25, L1-27, L1-42, L1-49, L1-50, L1-53, L1-56, L1-58, L1-63, L1-64, L1-66, L1-68, L1-90, L1-99
window accelerators R1-13
in XDM F2-6
window buttons R1-13
in XDM F2-5
Window Close command V2-4
Window menu
ViewDraw V/ApA-2
ViewWave V/ApC-1
Window Open Utility Workview Check Project command V3-7, V11-112, V12-8
Window Open Viewdraw Schematic command V3-1, V11-19, V11-27, V11-44, V11-66, V11-67, V11-88, V11-140, V12-6, V12-52, V16-12, V16-15, V16-39, V16-49, V/ApA-2
Window Open Viewdraw Symbol command V16-47, V/ApA-3
Window Open Viewfile command V2-3, V11-23, V16-12, V16-47
Window Open Viewsim command V12-12, V12-35, V12-52
Window Open Viewtext command V12-45, V12-46
Window Open Viewwave Savefile command V16-40, V/ApC-1
Window Open Viewwave Viewsim command V9-8, V12-14, V12-39, V12-52, V14-21, V14-26, V16-43, V/ApC-2
window operations R1-12
in XDM F2-5
window option A6-32
Window Push command V12-22, V12-26, V12-56
Window Close command V11-25, V11-30, V11-44, V11-66, V11-87, V12-28, V12-43, V16-12, V16-15, V16-40, V16-48, V/ApA-3
Window Close All command V/ApA-4
wir file A7-23, E5-3, F/ApC-23, V11-52
file-save command V/ApA-40
file-writeto command V/ApA-17
generating ViewDraw schematic with ViewGen V1-2, V10-1, V10-23, V10-25, V10-27, V/ApD-6, V/ApD-15, V/ApE-15, V/ApE-17, V/ApE-19
input to VSM V10-9, V10-10, V10-12, V10-15, V10-17, V10-19, V14-20
input to VSMUPD V10-21
input to WIR2XNF V7-6, V7-10, V11-148, V13-14, V13-19, V14-19
input to XEMake V7-10
input to XMake V7-2, V7-10, V11-1
inverter inserted by ViewBase V/ApE-4
library aliases V/ApF-2
multiple V10-28, V16-38, V/ApD-2
output by Check program V3-7, V11-1, V11-51, V11-52, V11-112, V12-8, V13-14, V14-19, V14-20, V/ApA-27, V/ApF-7
output by XNF2WIR V10-8, V10-10, V10-12, V10-17, V10-18, V13-15, V14-26, V16-38, V/ApD-2
overscores V3-2, V/ApA-21
re-creation by XSimMake V12-32
routed V10-21
simulation V14-21
translation to VSM file V10-8, V10-19, V12-9
unrouted V10-21
user-created libraries V3-8

wir subdirectory V2-2, V3-8, V6-2, V8-2, V8-3, V10-3, V10-8, V10-10, V10-17, V10-19, V10-25, V11-6, V11-9, V12-29, V/ApA-27, V/ApE-14
WIR2NET command F2-21, F5-15
WIR2XNF V10-8, V10-23
  accessing through XDM R1-22
  bus names V3-3
  checking pin/block connections V/ApD-18
  cross-reference file V/ApE-3, V/ApE-4
  error messages V/ApE-22
  expanding bus notation V3-3
  flattening macros and symbols V/ApD-17
  functional simulation V10-8
  inputs V10-3
  invalid characters V3-2
  invoking V10-3
  options
    -b V/ApD-18
    -c V/ApD-18
    -f V/ApD-17
    -od V/ApD-18
    -p V11-148, V/ApD-17, V/ApE-21, V/ApE-22
    -x V/ApD-2, V/ApD-17
  outputs V10-3, V10-23, V11-11
  purpose V10-3
  rule checking V10-3
  running with XEMake V7-7, V7-10, V16-33
  running with XMake V7-2, V7-6, V13-19, V14-23
  running with XSimMake V13-14, V14-19
  specifying output directory V/ApD-18
  specifying part type V/ApD-17
  suppressing output messages V/ApD-18
  warning messages V/ApE-20
WIRED style B4-34
Wired-AND
  ANDBUS WAND style B4-3
wirelist file F2-30, F2-31, F2-32
wires
  place O11-40, O16-18
  wire labels O16-23
Workview A7-18, A7-19, A7-20, A7-23, R1-60, V1-1, V1-2, V2-1
  changing menu structure V11-17
  changing XDM directory V2-4, V2-8
  configuring environment V2-1
  creating project V12-5, V13-2, V14-2, V15-3
  exiting V11-25, V12-28, V12-47, V12-56, V16-11, V16-28, V16-54
  file extensions V16-11
  function keys *see* function keys
  help V11-19
  invoking V11-15, V12-6, V12-33
  menu commands V11-19, V11-21
  mouse buttons *see* mouse buttons
  mouse configuration O16-12
  netlist, creating F2-21
  renaming schematics in DOS V16-28
  see also Viewlogic
Workview PLUS V1-1, V1-2, V2-1, V11-3, V12-3
workview.ini file V2-2, V11-16, V11-17
world view R3-78
WR_EN
  SRAM B4-107

## X

X attribute B6-5
X flag, *see* external flag
X net attribute L1-35, V4-10
X option A6-49
XABEL E1-3
  Compile menu
    PCs A6-6

XABEL, Compile menu *(Continued)*
workstations A6-32
definition A1-1, A1-6, A1-9
Edit menu
PCs A6-3
workstations A6-21
editing window A2-1
exiting A5-3, A5-9, A6-3, A6-21
File menu
PCs A6-1
workstations A6-19
help A2-6, A6-16, A6-36
Help menu
PCs A6-16
workstations A6-36
invoking from operating system A2-1, A5-1
invoking from XDM A2-1, A5-1
menus A2-3
opening new ABEL-HDL file A5-2
Options menu
PCs A6-15
workstations A6-23
PC commands A6-1
saving file and exiting A6-3
Show menu A6-34
View menu A6-5
workstation commands A6-19
XACT
directory structure O2-3
root directory F5-13, F/ApC-5
software directory F2-2
variable F/ApC-5
XACT Design Editor (XDE) M11-93, M15-29, R1-5, R3-53, V11-125, V15-30
checking design rules V11-129
exiting V11-130
finding blocks V11-128
highlighting nets V11-129
invoking V11-126
keyboard commands V11-129
XACT Design Editor, *see* XDE
XACT design flow R1-2
design entry R1-2
design implementation R1-2
design verification R1-3
XACT Design Manager A1-1, R1-3, U5-1
XACT Design Manager, see XDM
XACT Development System documentation *see* documentation
XACT environment R1-3, R1-4, R1-5
XACT environment variable V14-11, V16-5
XACT libraries M3-4, M3-5
XACT path O10-22
xact.pro file R3-68, R3-71
xactinit.dat files R2-188
xactinit.dat settings B/Ap-1, B/Ap-3
XACT-performance M15-1, O15-1, U2-5, U4-8
adding timing constraints
combining sets (TIMEGRP) O15-23
defining sets (TIMEGRP) O15-21
defining TNM groups O15-15
specific paths O15-15
TIMESPEC constraints O15-24
adding timing constraints to specific paths V15-13
adding TNM attribute to schematic V15-11
attributes B2-30, V4-9
auto R1-82
auto parameter R1-85
automatic delay R1-82
basic groups R1-70
basic path types R1-86
c2p R1-86
c2s R1-86
clock–to–pad paths R1-89
clock–to–setup paths R1-86
combinational loops R1-82
combining multiple groups R1-78

XACT-performance *(Continued)*
computing delays V15-1
concepts O15-3
creating a routed design with XMake V15-23
creating Workview project directory V15-3
defining sets with TNM attribute V15-14
default timing specifications O15-12, R1-72, R1-85
devices supported V15-1
difference between path–type and end–point specifications R1-102
disabling paths O15-36
entering default timing specifications V15-11
evaluating results (XDelay)
Failedspec option O15-39
SelectSpec option O15-39
examining PPR errors V15-24
EXCEPT statement O15-7
FALLING keyword R1-79
forward tracing R1-93
From–To statement R1-71
group by clock sense R1-79
group by exclusion R1-79
group by signal name R1-79, R1-80
grouping sets with TIMEGRP symbol V15-17
grouping symbols O15-6
guided design R2-183
ignore R1-101
ignore selected paths R1-81
ignore value V15-10
ignoring a path R1-101
interaction with PPR V15-9
LINK R1-100
logic primitives B2-32
multiple specifications R1-81
new groups from existing groups R1-77
overlapping specifications R1-81, R1-92
p2p R1-86
p2s R1-86
pad–to–pad paths R1-90
pad–to–setup paths R1-88
parameters R2-29, R2-32, R2-36, R2-37, R2-39
path–type specifications R1-85
path–type timing specifications
sample schematic R1-101
pattern matching R1-79
predefined groups R1-72
purpose V15-1
RISING keyword R1-79
sample schematic R1-84
setting default timing requirements V15-10
specifying requirements in PPR R2-195
specifying timing constraints with TIMESPEC symbol V15-19
syntax V15-4
TIMEGRP attributes R1-77
flip-flops by clock edge O15-8
TIMEGRP primitive R1-77
TIMEGRP symbol, *see* TIMEGRP symbol
TIMESPEC attribute O15-9
TIMESPEC primitive R1-70
TIMESPEC symbol, *see* TIMESPEC symbol
TNM attribute, *see* TNM attribute
TNMs R1-73
TS attribute R1-70
placement R1-72
TS flags R1-94
tutorial M15-1
adding TNM M15-10
ALUFF class M15-15
analyze mode M15-31

XACT-performance, tutorial *(Continued)*
analyze mode output M15-31
analyzing design M15-29
clock speed M15-11
ClockToPad option M15-28, M15-38
ClockToSetup option M15-28, M15-38
CTLFF class M15-16
default timing M15-9, M15-11
EditLCA M15-41
EXCEPT statement M15-6
FailedSpec option M15-28, M15-32
flagblk option M15-27, M15-29
floorplanning M15-9
FromFF option M15-28, M15-40
grouping symbols M15-3
ignore value M15-9
implementation M15-22
INFFS class M15-14
installing M15-2
maxpaths M15-39
PadToPad M15-38
PadToPad option M15-28
PadToSetup option M15-28, M15-38
PLD_Men2XNF8 M15-23
PLD_XMake M15-23
PLD_XMake output M15-23
PPR M15-1, M15-8, M15-22
PPR log file M15-24
predefined class M15-5
query template M15-30
required software M15-2
running XDelay M15-29
SD/RD pins M15-30
SelectSpec option M15-28, M15-32
speed grade M15-9
stacker class M15-14
STFF class M15-16
TIMEGRP M15-3, M15-5, M15-17
TIMESPEC M15-3, M15-7, M15-11
TIMESPEC constraints M15-19
TIMESPEC mode M15-32
TIMESPEC output M15-33
timing constraints M15-8, M15-13
timing specifications M15-7
TNM attribute M15-3
TNM groups M15-14
ToFF option M15-28, M15-40
TSMaxpaths option M15-33
using XACT-Performance M15-8
XDelay M15-1, M15-27
XDelay mode M15-38
XNFPrep M15-24
XRP file M15-37
tutorial files V15-2
viewdraw.ini file V15-3
when to use V15-9
XACTUSER environment variable R1-8
XAS file A1-6, A1-8, A5-5, A5-7, M3-9, V6-10, V14-10, V14-19
X-BLOX M1-8, M3-4, M10-3, M10-7, R1-40, R2-184, U2-2, U5-4, U5-5
accessing through XDM R1-22
adding a bus O13-6
adding elements to ViewDraw schematic V13-6
adding module to schematic O13-3
adding module to ViewDraw schematic V13-3
attributes V6-8, V13-7, V13-9
buses O13-6, O13-8, V4-16, V6-8, V12-34, V13-6, V13-7, V13-9, V13-13, V13-16
BOUNDS attribute O13-7
ENCODING attribute O13-7
creating a design O13-5
creating routed design with XMake V7-6, V13-18, V13-20

X-BLOX *(Continued)*
creating Workview project directory V13-2
elements R1-116
examining XSimMake output V13-14, V13-22
features B1-1
block-diagram design B1-1
compatibility B1-2
data path B1-1
optimization B1-2
functional simulation M6-6, O13-11, V1-3, V6-7, V6-10, V10-5, V10-6, V10-9, V12-28, V12-29, V13-11, V13-16
functional simulation *see also* functional simulation V6-3
implementation O13-17
in XNFPrep design flow R2-29, R2-31, R2-35
inputs and outputs R2-32, R2-34
library M3-4, M13-1, M13-8, O13-10, V3-5, V4-16, V13-1, V13-3, V13-10
macros V13-10, V13-11, V13-18
optimization M7-3
options
archopt B/Ap-1
blxfile B/Ap-1
mergeio B/Ap-2
modgen B/Ap-2
parttype B/Ap-2
sim B/Ap-2
simdir B/Ap-2
subscripts B/Ap-2
syntax B/Ap-1
program description M10-29
schematics V13-11
simulation schematics V12-33
simulating a design O13-15, O13-22
timing simulation O13-20
symbols R2-32, R2-36, R2-40, R2-41, V1-3, V4-16, V13-16, V13-20
ACCUM B4-8
ADD_SUB B4-14, V13-10
ANDBUS B4-4, V13-10
ANDBUS1 B4-4
ANDBUS2 B4-4
BIDIR_IO B4-18
BUS_DEF B4-22, O13-7
BUS_IFxx B2-28
CAST B4-24
CLK_DIV B4-28
COMPARE B4-32
COUNTER B4-36
DATA_REG B4-48, V13-10
DECODE B4-58
ELEMENT B4-60
FORCE B4-62
functional simulation O10-13
INC_DEC B4-64
INPUTS B4-68
INVBUS B4-5
MUXBUS B4-72, V13-10
MUXBUS2 B4-74
MUXBUS4 B4-76
MUXBUS8 B4-78
ORBUS B4-5, V13-10
ORBUS1 B4-6
ORBUS2 B4-6
OUTPUTS B4-80
PROM B4-84
SHIFT B4-92
SLICE B4-102
SRAM B4-106
TRISTATE B4-110
XORBUS1 B4-7, V13-10
XORBUS2 B4-6, B4-7
syntax M10-29
timing simulation M8-3, V1-3, V12-49, V13-21, V13-23
timing simulation *see also* timing simulation V8-2

X-BLOX *(Continued)*
tutorial M13-1
ADD_SUB M13-9
adding X-BLOX module M13-3
ANDBUS M13-9
ASYNC_VAL M13-8
back-annotation M13-21
BLOXSOLN M13-11, M13-13
BOUNDS attribute M13-6
bus definition M13-7
bus widths M13-6
BUS_DEF M13-6
BUS_IF symbol M13-6
buses M13-5
completing ALU_BLOX M13-5
DATA_REG M13-8
design description M13-2
do file M13-17, M13-24
download to demo board M13-20
ENCODING attribute M13-6
FNCSIM8 output M13-13
functional simulation M13-10
Gen_Sch8 M13-13
implementation M13-18
INVMASK M13-9
library M13-1, M13-8
Men2xnf8.log file M13-11
MUXBUSx M13-9
ORBUS M13-9
PLD_FNCSIM8 M13-9, M13-10, M13-13
PLD_Men2XNF8 M13-11
PLD_TIMSIM8 M13-21
PLD_TIMSIM8 output M13-21
PLD_XMake M13-9, M13-18
PLD_XMake output M13-18
QuickSim II M13-17, M13-23
required software M13-1
SIMDIR M13-10
symbols M13-8
SYNC_VAL M13-8
timing simulation M13-21
TIMSIM8 M13-21
viewing ALU_BLOX M13-3
viewing schematic M13-15
XBLXGS M13-10, M13-13
tutorial files V13-2
variables M10-29
VHDL V1-2
viewdraw.ini file V11-8, V13-3
XC3000A/L PPR design flow R2-172
XC3100A PPR design flow R2-172
XC4000 PPR design flow R2-170
XMake output O13-18
XSimMake output (functional) O13-12
XSimMake output (timing) O13-21
XBLXGS M10-7, M10-11
error messages M/Ap-9
options M10-31
syntax M10-30
variables M10-30
XC2000 designs U1-4, U1-8, U5-1
library aliases V2-12
mapping all macros in XMake R1-39
placing and routing R1-4
XC2000/XC3000 designs
globalresetb M9-2, M9-5
XC2000L U1-4, U1-8, U5-1
XC3000 Demonstration Board
description H1-4
operation H1-9
creating design for download H1-9
using download cable H1-9
using with PROM H1-12
purpose H1-1
requirements to operate H1-1
using with sample design H1-14
XC3000 designs U1-3, U1-7, U5-1
demonstration board V11-88, V11-92, V11-93, V11-130, V11-131, V11-134
library aliases V2-12
oscillator O11-49

XC3000 designs *(Continued)*
placing and routing R1-4
unconvertible symbols V/ApF-7
using as basis for XC4000 design V/ApF-7
XC3000A U1-3, U1-7, U5-3
XC3000A/L designs
constraints in guided design R2-184
guided design R2-177, R2-184
PPR design flow R2-168
PPR design flow with X-BLOX R2-172
XC3000L U1-3, U1-7, U5-3
XC3100 U1-3, U1-7, U5-1
XC3100A U1-3, U1-7, U5-3
XC3100A designs
constraints in guided design R2-184
guided design R2-177, R2-184
PPR design flow with X-BLOX R2-172
XC4000 Demonstration Board V11-90, V11-92, V11-130, V11-131, V11-134
components H2-2
5-volt power connector H2-5
alternate power connector power connector H2-5
configuration switches H2-11
crystal oscillator H2-12
LED indicators H2-10
mode pins H2-12
multiple program enable H2-11
Octal DIP switch H2-9
power switch H2-11
PROG push button H2-9
RESET push button H2-8
reset switch H2-12
seven-segment displays H2-10
single program enable H2-12
SPARE push button H2-10
XChecker connector H2-6
description H2-2
downloading with XChecker H2-13
example of usage H2-15
loading with configuration PROM H2-14
purpose H2-1
requirements to operate H2-2
XC4000 designs U1-5, U5-4
constraints in guided design R2-184
globalsetreset M9-2, M9-5
guided design R2-177
ignoring FMAP and HMAP symbols R2-205, R2-217
library aliases V2-12
oscillator O11-51
placing and routing R1-5
PPR design flow R2-167
PPR design flow with X-BLOX R2-170
RAM data values R1-62
running X-BLOX in XMake R1-40
using XC3000 as design basis V/ApF-7
XC4000A U1-5, U5-4
XC4000H U1-6, U5-4
XC4000H output driver L1-6
XC7000 devices F/ApC-9, F/ApC-10
XC7000 library M3-10, M5-1, V2-12, V5-1, V5-10, V5-12, V5-14
XC7200 and XC7300 devices F2-17
XChecker V7-1, V11-14, V11-131, V11-135, V11-146
accessing through XDM R1-28
baud rates H5-4
cable H1-1, H1-4, H1-5, H1-9, U1-13, U4-9
XC4000 Demonstration Board H2-1, H2-2, H2-6
in slave-serial mode U6-20
using BIT file U6-3
cable connections H5-13, H5-14, O11-88
communications guidelines H5-56
connecting cable H5-11
checking cable H5-12

XChecker *(Continued)*
- connecting for asynchronous probing H5-22
- connecting for download H5-17
- connecting for synchronous probing H5-20
- connecting for verification H5-18
- connecting to host system H5-11
- connecting to target system H5-13

connecting control signals to VCC and ground H5-58
creating downloadable design H5-9
design verification O11-86
displaying readback data in Viewlogic H5-40
downloading H5-25
error messages H5-60
files used H5-23
generating configuration bitstream H5-10
hardware H5-1
improper connections H5-57
invoking H5-25
operation mode connections H5-17
options
- command line H5-41
  - displaying help H5-42
  - executing batch file H5-41
  - specifying part type H5-42
  - specifying port names H5-42
  - verifying download and readback H5-42
- interactive mode
  - checking cable hardware H5-46
  - displaying data read back H5-53
  - displaying help H5-47
  - displaying option settings H5-52
  - displaying pin logic level H5-54
  - displaying show command data H5-45

displaying signal data horizontally H5-53
displaying signal data vertically H5-53
downloading design to LCA H5-47
executing batch file H5-43
exiting XChecker H5-46, H5-51
expanding search for matching file names H5-48
listing matching file names H5-48
naming screen output file H5-48
naming signal group H5-47
reading back data snapshots H5-51
resetting LCA before readback H5-55
resetting LCA internal logic H5-52
retrieving data H5-47
saving option settings H5-52
saving readback data to file H5-46
saving readback data to Viewlogic file H5-46
saving screen output to file H5-48
selecting readback trigger H5-54
selecting signals displayed by show command H5-49
selecting signals to display H5-53
selecting snapshots to display H5-53
setting maximum number of data snapshots H5-52
specifying baud rate H5-43

XChecker, options *(Continued)*
specifying clock source H5-44
specifying download/read-back port H5-50
specifying part type H5-48
specifying signals to be probed H5-50
suspending XChecker H5-54
verifying download and read-back H5-48
verifying target LCA bitstream H5-56
probing internal logic
XC2000 and XC3000 designs H5-28
XC4000 designs
asynchronous probing H5-37
synchronous probing H5-32
purpose H5-1
RAM bits in XC4000 H5-38
requirements for use H5-5
using with non-XChecker download cables H5-4
verifying configuration H5-26
warning messages H5-58
xchecker.pro file V11-135, V11-146
FPGA Demonstration Board H3-26
XC4000 Demonstration Board H2-14
XDE L1-20, L1-35, M11-93, O11-82, R2-175, R2-177, R2-182, R2-195, R2-227, R3-29, U3-3, U3-7, U4-5, U5-3, U6-1, U8-14
accessing MakePROM R2-270, R2-273
accessing through XDM R1-24
activating readback U7-9
bitstreams
creating in LCA file R3-145
downloading to cable R3-119, R3-124
reading file R3-168
saving current configuration R3-193
blocks
assigning names R3-150
coloring R3-104
configuring logic and connections R3-105
copying configuration R3-114
deconfiguring R3-103, R3-120
deselecting R3-130
displaying configuration information R3-102
displaying information on saved blocks R3-168
displaying scrolling menus R3-102
editing comment text R3-126
flagging for path delay calculator R3-138
highlighting connections R3-185
moving configuration and net connections R3-148
moving window to R3-137
removing connections from world view R3-192
requesting information R3-159
restoring saved information R3-171
routing pins R3-172
saving in temporary space R3-175
saving information to text file R3-171
swapping R3-188
swapping net connections R3-186
tagging with text R3-104
unrouting pins R3-191
checking design rules M11-96
CLBs
configuring carry logic function R3-113
configuring logic functions R3-132
ordering logic function inputs R3-152
setting constraint file flag R3-146

XDE *(Continued)*
commands
adding delay to clock paths R3-177
adding pin to net R3-96
altering net routing R3-127
assigning block name R3-150
assigning color to Block Editor display R3-100
assigning internal net to predefined probe R3-97
assigning IOB name R3-119
assigning net to pin within block R3-97
assigning routing weight to net R3-193
changing base configuration R3-99
changing cursor shape R3-115
changing editor item color R3-154
changing from PIE to Block Editor display R3-190
changing mouse configuration R3-147
changing width of highlight lines R3-142
clearing CLB and IOB tags R3-103
clearing margin delays R3-103
clearing XDelay options R3-104
coloring blocks R3-104
coloring nets R3-105
configuring CLB carry logic R3-113
configuring CLB logic function R3-132
configuring interconnects for net R3-172
configuring pin interconnects R3-172
copying block configuration R3-114
creating and downloading bitstream R3-119
creating bitstream of LCA file R3-145
creating net R3-95
creating printable file R3-124, R3-157
deconfiguring blocks R3-103, R3-120
deconfiguring net interconnects R3-191
deconfiguring pin interconnects R3-191
defining function keys R3-143
deleting net R3-122
deleting pin R3-122
deselecting current block R3-130
displaying block configuration information R3-102
displaying block name menu R3-102
displaying editor settings R3-178
displaying grid information R3-163
displaying help R3-141
displaying list of probes R3-166, R3-168
displaying net information R3-163
displaying net menu R3-152
displaying options R3-168
dissociating logical name from IOB R3-190
dissociating probe from internal net R3-190
downloading bitstream to cable R3-124
editing block comment text R3-126
editing equations R3-126
enabling Prtsc key R3-131
entering equations in Block Editor R3-132
executing command file commands R3-133

XDE, commands *(Continued)*
executing cut file commands R3-154
executing macro file commands R3-144
exiting command file R3-131
exiting XDE and saving design R3-136
exiting XDE without saving design R3-135
flagging blocks for delay calculator R3-138
flagging CLBs/IOBs for constraints R3-146
flagging I/O blocks for internal/external use R3-140
flagging net with attributes R3-140
flagging nets for constraints R3-146
flagging pins for constraints R3-146
highlighting block connections R3-185
highlighting net interconnects R3-141
highlighting nets R3-185
highlighting nets after modification R3-192
interchanging pin functionality R3-188
invoking Block Editor R3-125
invoking DRC R3-125
merging nets R3-143
moving block internal configuration R3-148
moving configuration R3-115
moving pin net connection to other pin R3-148
moving window R3-136
moving window to block R3-137
moving window to net R3-137
moving window to pin R3-137
ordering CLB logic function R3-152
reading bitstream file R3-168
reading constraint file R3-169
reading margin delay file R3-169
reading probe set into LCA file R3-169
reading schematic constraint file R3-170
reading XDelay option file R3-170
refreshing display R3-171
removing block connections from world view R3-192
removing highlighting from net interconnect R3-191
removing net connections from world view R3-192
renaming net R3-152
reporting LCA timing information R3-194
reporting path delays R3-165
requesting block data R3-159
restoring saved information to block R3-171
routing all block pins R3-172
routing along specified path R3-173
saving block in temporary space R3-175
saving block/net information in text file R3-171
saving configuration macro R3-116
saving current bitstream R3-193
saving current design state R3-175
saving margin delays to file R3-175
saving options to editlca.pro file R3-176
saving probes to PRB file R3-176
saving XDelay options to file R3-177
selecting port for download R3-154

XDE, commands *(Continued)*
selecting status line format R3-186
setting configuration tags R3-105
setting device speed grade R3-185
setting MakeBits configuration tags R3-114
setting options in editlca.pro file R3-170
setting printer type R3-158
setting routing costs R3-173
snapping pins or PIPs to cursor R3-185
splitting nets R3-186
storing values in CLB ROM R3-178
suspending XDE R3-122
swapping block net configurations and connections R3-186
swapping groups of blocks R3-188
tagging block with text R3-104
turning automatic routing off and on R3-98
turning automatic timing off and on R3-99
turning DRC off and on R3-98
unrouting block pins R3-191
updating option display R3-178
writing constraint information to file R3-194
configuration tags
XC2000 R3-106
XC2000 CLBs R3-109
XC2000 IOBs R3-111
XC3000 CLBs R3-109
XC3000 IOBs R3-111
XC4000 R3-108
XC4000 CLBs R3-110
XC4000 IOBs R3-112
constraints
reading file R3-169
reading schematic file R3-170
setting file flag for CLBs/IOBs R3-146
setting file flag for nets R3-146
setting file flag for pins R3-146
writing to file R3-194
design editor
abbreviations R3-92
block editor R3-77, R3-86, R3-100, R3-125, R3-126, R3-132, R3-190
tags R3-90
XC3000 CLB and IOB R3-88
XC4000 CLB and IOB R3-89
block names R3-92
default values R3-91
entering commands R3-91
parameter selection R3-91
physical interconnect editor R3-78, R3-190
command line R3-78, R3-86
cursor R3-78, R3-85
cursor-status line R3-78, R3-85
LCA layout R3-78, R3-79
message line R3-78, R3-86
pulldown menus R3-78, R3-86
world view R3-78
pin names R3-92
purpose R3-77
wildcards R3-92
EditLCA screen O11-84
executive
commands R3-56
changing menu colors R3-65
changing name of current design file R3-67
choosing menu commands with arrow keys R3-63
converting device to other part type R3-58
defining function keys R3-64
displaying option settings R3-72

XDE, executive, commands *(Continued)*
enabling fast writing and reading R3-62
entering DOS temporarily R3-60
executing command sequence R3-61
exiting XACT R3-70
invoking Design Editor R3-61
invoking DRC R3-61
invoking MakeBits R3-65
invoking MakePROM R3-65
loading settings from xact.pro file R3-71
obtaining help on editor commands R3-63
printing PIC file R3-70
reading palettes.xct file R3-70
save option settings in xact.pro file R3-71
saving current design state R3-71
saving design and exiting XACT R3-63
selecting color palette R3-67
selecting device spped grade R3-72
selecting DIE or PKG file for design R3-67
selecting printer type R3-68
setting current directory R3-60
setting cursor shape R3-59
setting mouse configuration R3-66
setting safe mode R3-65
specifying current design file R3-60
specifying file to load R3-70
display R3-53
exiting XACT R3-57
loading and saving design files R3-56
options R3-54
printcap.xct file R3-73, R3-75
printer commands R3-73
purpose R3-53
starting XACT subprograms R3-56
syntax R3-53
unsupported printers R3-72
display screen U9-2
finding block M11-95
guided design R2-175, R2-180
highlighting net M11-96
invoking M11-93
IOBs
dissociating logical names R3-190
flagging for internal/external use R3-140
naming as probe R3-119
setting constraint file flag R3-146
macros
creating for multiple instances R3-116
margin delays
clearing R3-103
reading from MRG file R3-169
saving R3-175
nets
adding R3-95
adding pins R3-96
altering routing R3-127
assigning routing weight R3-193
assigning to pins R3-97
assigning to predefined probe R3-97
coloring R3-105
coloring interconnects R3-141
configuring interconnects R3-172
deconfiguring interconnects R3-191
deleting R3-122
deleting pins R3-120

XDE, nets *(Continued)*
displaying information R3-163
displaying scrollilng menus R3-152
dissociating from probes R3-190
flagging with attributes R3-140
highlighting R3-185, R3-192
merging R3-143
moving connections between blocks R3-148
moving window to R3-137
removing connections from world view R3-192
removing highlighting R3-191
renaming R3-152
saving information to text file R3-171
setting constraint file flag R3-146
splitting R3-186
swapping connections on blocks R3-186
pins
adding to net R3-96
assigning nets R3-97
changing functionality R3-188
configuring interconnects R3-172
deconfiguring interconnects R3-191
deleting R3-122
deleting from nets R3-120
moving net connection R3-148
moving window to R3-137
routing on block R3-172
setting constraint file flag R3-146
snapping to cursor R3-185
unrouting on block R3-191
probe command U4-10
probes
assigning nets R3-97
printing list R3-166
reading into LCA file R3-169
saving to PRB file R3-176
purpose R1-5
representing internal CLB nodes R2-176
ROMs
setting default values R3-178
syntax R3-94
timing R3-194
tutorial U9-1
add nets to design U9-57
beginning U9-2
building a four-bit multiplier U9-45
choosing design file U9-4
ColorNet U9-44
connect pins U9-34
direct interconnect U9-28
disable Autoroute U9-33
downloading a bitstream U9-63
EditBlk screen U9-10
EditNet U9-44
exiting U9-64
function keys U9-8
general purpose interconnect U9-30
getting started U9-2
high-level editing U9-16
Hilight U9-44
improve routing U9-61
loading the design U9-5
logical block names U9-56
longlines U9-31, U9-40
low-level editing U9-23
manual routing U9-33
mouse buttons U9-7
new design U9-48
PIPs U9-27
QueryNet U9-18, U9-42
quitting U9-64
Route U9-43, U9-44
route nets U9-60
RoutePin U9-43
RoutePoint U9-44

XDE, tutorial *(Continued)*
screen options U9-25
setting the directory U9-4
setting the mode U9-3
setting the profile U9-7
Show Matrix option U9-26
similar commands U9-42
SwapBlk command U9-20
SwapSig command U9-16
switch matrix U9-34
Unroute U9-42
UnroutePin U9-42
viewing FPGA U9-5
world view U9-6
XDelay U9-61
xdefaults file F2-4, R1-12
XDelay M10-15, M10-16, M15-1, M15-27, R3-194, U4-5, U4-6, U9-61, V13-20, V13-22, V15-25
accessing through XDM R1-28
adding delay to clock path R3-17
analyzing best-case timing R3-15
analyzing worst-case timing R3-14
BreakLoop option
using for combinatorial logic R3-25
changing directory without exiting R3-2
changing displayed path order R3-14
changing speed grade R3-15
clearing all destination clocks R3-8
clearing all net filters R3-8
clearing all source clocks R3-7
clearing defined ignorenet statements R3-8
clearing margin delays R3-18
clearing options in XDE R3-104
clearing previously defined options R3-17
clearing synchronous outputs R3-20
clearing XDelay command options R3-14
ClearOptions command V15-40
command line options
displaying long timing report R3-25
displaying short timing report R3-24
exiting from XDelay R3-24
obtaining help R3-24
rewriting LCA file after timing R3-25
sending delay report to file R3-24
setting speed grade R3-25
using path-tracing options in template file R3-24
command line syntax R3-24
creating output file R3-21
creating TimeGroups R3-15
-d option R3-24
defining function keys R3-23
defining mouse buttons R3-23
deleting specified groups R3-16
deleting TimeSpecs set in R3-17
Design menu R3-2
Design command R3-3
directory command R3-2
displaying help text R3-20
displaying options R3-23
displaying options in XDE R3-168
exiting XDelay R3-21
filtering paths with certain nets R3-8
flagging blocks for path delay R3-18
FromAll option V15-43
function generators R3-20
getting a list of elements in a delay group R3-16
graphical interface R3-2
ignoring paths through specified nets R3-8
including unspecified paths in report R3-7
invoking V15-30

XDelay *(Continued)*
limiting number of paths for TimeSpecs R3-13
limiting number of paths printed in report R3-13
limiting number of report characters per line R3-14
listing currently defined TimeSpecs R3-17
listing defined options R3-17
marking nets as synchronous sources R3-8
Misc menu R3-20
DOS command R3-21
Execute command R3-21
Exit command R3-21
Help command R3-20
Print command R3-21
Printer command R3-21
Report command R3-21
modes
analyze V15-28, V15-31
XDelay V15-28, V15-39
XDelay-TimeSpec V15-28, V15-33
-o option R3-24
obtaining design timing information R3-3
obtaining timing information from XDE R3-194
options
clear template V15-28, V15-31
ClearOptions V15-33
ClockToPad V15-29, V15-39
ClockToSetup V15-29, V15-39, V15-40
-dw V10-14
FailedSpec V15-28, V15-33
flagblk V15-28, V15-30, V15-34
From V15-43
FromFF V15-29, V15-41
FromIOB V15-43
maxpaths V15-40
PadToPad V15-29, V15-39
PadToSetup V15-39
query template V15-28, V15-31
read template V15-28, V15-31
save template V15-28, V15-31
SelectSpec V15-28, V15-33
To V15-43
ToAll V15-43
ToFF V15-29, V15-41
ToIOB V15-43
TSMaxpaths V15-28, V15-34
path delay searches R3-26
printing delay path summaries R3-14
printing paths that fail timing specifications R3-7
Profile menu R3-22
Cursor command R3-23
Keycursor command R3-23
Keydef command R3-23
Mouse command R3-23
Palette command R3-23
Readprofile command R3-23
Saveprofile command R3-23
Settings command R3-23
program description M10-31
purpose R1-5, R3-1, V14-25, V15-1, V15-28
reading margin definitions R3-18
reading option definitions from template file R3-17
reading option file in XDE R3-170
reading option settings from xdelay.pro file R3-23
removing existing BreakLoops R3-8
report file V15-40
reporting added path delay R3-18
reporting on blocks R3-20
reporting on nets R3-20
reporting only combinatorial paths R3-9

XDelay *(Continued)*
- reporting paths ending at clock pins R3-13
- reporting paths ending at clocked elements R3-9
- reporting paths starting at clocked elements R3-10
- reporting paths starting at clocked outputs R3-11
- running batch file R3-21
- running template files in batch mode R3-23
- running with XMake V14-23
- -s option R3-24
- saving option definitions to a template file R3-17
- saving option settings to file R3-23
- saving options in XDE R3-177
- selecting cursor shape R3-23
- selecting design to load R3-3
- selecting menu colors R3-23
- selecting printer file format R3-21
- setting clock net as ending point for path searches R3-7
- setting clock net as starting point for path searches R3-7
- setting enviromental variables for R3-27
- setting maximum path delay for reported paths R3-13
- setting minimum path delay for reported paths R3-13
- setting timing specifications for paths R3-16
- specifying all destinations as ending point for path delay R3-7
- specifying all sources as starting points for path delay R3-6
- specifying ending point for path delay R3-6
- specifying flip-flops as ending point for path delay R3-6
- specifying flip-flops as starting point for path delay R3-6
- specifying function generators as starting points for path delay R3-20
- specifying IOBs as ending point for path delay R3-6
- specifying IOBs as starting point for path delay R3-6
- specifying starting point for path delay R3-6
- starting DRC R3-20
- starting graphical interface R3-24
- suspending XDelay R3-21
- -t option R3-24
- Text Interface R3-23
- TimeGroups R3-25
- timing margins R3-27
- Timing menu R3-3
  - ClearMargins command R3-18
  - ClearTemplate command R3-17
  - DeleteGroup command R3-16
  - DeleteSpec command R3-17
  - DRC command R3-20
  - FlagBlk command R3-18
  - QueryBlk command R3-20
  - QueryGroup command R3-16
  - QueryMargins command R3-18
  - QueryNet command R3-20
  - QuerySpec command R3-17
  - QueryTemplate command R3-17
  - ReadMargins command R3-18
  - ReadTemplate command R3-17
  - Savemargins command R3-18
  - SaveTemplate command R3-17
  - SetMargins command R3-17
  - Speed command R3-15
  - TimeGroup command R3-15
  - TimeSpec command R3-16
  - XDelay command R3-3
    - padToSetup option R3-9

XDelay *(Continued)*
-u option R3-25
using arrow keys in menu R3-23
using -FailedPaths option with TimeSpec command R3-16
using -FailedSpec option with Time-Groups R3-25
using timing specifications R3-7
using within XDE R3-2
valid TimeGroups, described R3-15
-w option R3-25
writing delays into LCA file with XMake V7-6
writing print file of screen R3-21
-x option R3-25
XDELAY_MAX_PATHS variable R3-28
XDELAY_PRECISION variable R3-27
XDelay ClearOptions command O15-46
XDelay command
-Analyze option R3-15
-BreakLoop option R3-8
-ClearOptions option O15-46, R13-14
-ClockInput option R3-13
-ClockToPad option R3-10
-ClockToSetup option R3-10
-Delaygreater option R3-13
-Delayless option R3-13
-DestClock option R3-7
-FailedSpec option R3-7
-From option R3-6
-FromAll option R3-6
-FromFF option R3-6
-FromIOB option R3-6
-Ignorenet option R3-8
-Maxpaths option R3-13
-Netfilter option R3-8
-NoBreakLoop option R3-8
-NoDestClock option R3-8
-NoIgnorenet option R3-8
-NoNetfilter option R3-8
-NoSourceClock option R3-7
-PadToPad option R3-9
-Shortreport option R3-14
-Sort option R3-14
-SourceClock option R3-7
-TimeSpec option R3-7
-To option R3-6
-ToAll option R3-7
-ToFF option R3-6
-ToIOB option R3-6
-TSMaxpaths option R3-13
-Unspecified option R3-7
-Widereport option R3-14
-WorstCase option R3-14
XDelay program O10-16, O15-34
analyze mode O15-37
invoking O15-36
XDelay-TimeSpec output O15-40
xdelay.pro file R3-23
XDELAY_MAX_PATHS variable R3-28
XDELAY_PRECISION variable
in XDelay R3-27
XDELAY-TIMESPEC mode V15-33
XDM A1-1, E3-7, F2-1, M1-7, U5-1, V12-2, V12-3, V13-1, V14-1, V15-2
accessing R1-9
accessing text editor from XDM F/ . ApC-10, O16-9
adding to path V16-5
changing menu colors R1-33
changing mouse button function R1-33
command entry F2-8
command line interface F2-9, R1-18
configuration O11-69
configuring the environment F/ApC-9
configuring XMake V11-114
customizing interface V16-10
customizing screen color R1-34
defining function keys R1-33
Design Entry Menu
SYMGEN R1-19

XDM *(Continued)*
DesignEntry menu V2-13, V11-16, V11-140, V12-33, V16-11
determining device family R1-32
displaying help R1-7
displaying installed Xilinx programs R1-32
displaying profile configuration R1-34
displaying settings of F2-40
executable files R1-8
executing command files R1-31
exiting F2-3, V11-147
file extensions V16-11
Fitter menu
FITEQN R1-25
FITNET R1-25
PALCONVT R1-25
graphic interface F2-9, F/ApC-8, R1-18
handling unexpected results F/ApC-8
help F2-36, R1-31, V11-15
invoking V2-13, V11-15, V12-6
invoking ABL2PLD A5-8
invoking ABL2XNF A5-7
invoking Check program V11-113
invoking HM2RPM R1-117
invoking JED2HDLX A8-2
invoking PPR R2-186
invoking VSM V10-19
invoking VSMUPD V10-21
invoking Workview V2-12, V11-15, V12-6
invoking XABEL A1-6, A2-1, A5-1, A9-26
invoking XDE V11-126
invoking XNF2WIR V10-17
invoking XNFPrep R2-34
invoking XSimMake V6-5
JED2PLD command A7-5
main menu F2-3, F/ApC-6, F/ApC-7
main screen R1-10, R1-16
managing design directories R1-30
menu bar R1-10, R1-16
menus F2-16
Design Entry F2-18, R1-19
Fitter R1-24
Part V5-20
PC V16-7
Place Route F2-24, R1-23, V10-2, V11-126
APR R1-24
APRLoop R1-24
PPR R1-24
XDE R1-24
Profile F2-17, R1-19, R1-32
cursor command R1-32
family command R1-32
KeyCursor command R1-33
keydef command R1-33
Menucolors command R1-33
Mouse command R1-33
Options command R1-33
Palette command R1-34
Part command R1-34
Readprofile command R1-34
Saveprofile command R1-34
Settings command R1-34
Speed command R1-34
Translate F2-18, R1-19, V5-13, V5-16, V7-4, V7-8, V7-13, V7-14, V10-2, V11-118, V11-145
ABL2PLD R1-20
ABL2XNF R1-20
Anotate R1-20
cleanup R1-21
HM2RPM R1-21
INET R1-21
JED2PLD R1-21
MAP2LCA R1-21
MemGen R1-21
PinSave R1-22
PLUSASM R1-22
SDT2XNF R1-22

XDM, menus, Translate *(Continued)*
SYN2XNF R1-22
WIR2XNF R1-22
X-BLOX R1-22
XDRAFT R1-23
XEMake R1-20
XMake R1-20
XNFMAP R1-23
XNFMerge R1-23
XNFPrep R1-23
Utilities F2-17, F2-33, R1-19, R1-29, V12-31, V12-50
browse R1-29
DirClean R1-30
directory R1-30
DOS command R1-30
edit command R1-30
execute command R1-31
help command R1-31
report command R1-31
ScanDisk command R1-31
version command R1-32
Verify F2-28, R1-26, R2-273, V8-4, V10-2, V10-19, V10-21, V10-22, V11-135, V12-30, V12-49, V15-30, V16-37
ASCTOVST R1-26
LCA2XNF R1-26
MakeBits R1-26
MAKEJED R1-26
MAKEPRG R1-26
MakePROM R1-27
ORCAD (VST) R1-27
PROLINK R1-27
VMH2XNF R1-27
VSM R1-27
XChecker R1-28
XDelay R1-28
XNF2VST R1-28
XNF2WIR R1-29
XNFBA R1-28
XNFCVT R1-28
XPP R1-29
XSimMake R1-28
Workstation V16-8
display R1-19
mouse configuration F2-9, F/ApC-8, R1-18
moving cursor through menus R1-33
navigating through directories R1-30
opening screen
Directory field R1-16
Family field R1-16
Mouse field R1-16
Part field R1-16
opening screen, PCs
Directory field R1-11
Family field R1-11
Mouse field R1-11
Part field R1-11
opening screen, workstations
Command Line R1-14
Instruction Line R1-14
Status Line R1-14
overview of F1-2
path statement for F2-2, F2-4
PC systems R1-9
menu display R1-19
obtaining help R1-8
proglist.xdm file F2-6, R1-8, R1-14
purpose R1-3, R1-7, V11-1, V11-14, V12-5
quitting F2-3, F/ApC-6
reading profile saved in xdm.pro file R1-34
redirecting output to text file R1-31
running PRO Series for Windows V11-3
saving profile to xdm.pro file R1-34
saving settings F2-40
scanning hard disk drive R1-31
selecting default part type R1-34

XDM *(Continued)*
selecting software default options R1-33
selecting speed grade R1-34
setting cursor type R1-32
setting default options V11-115
specifying part type V11-93
specifying text editor V16-6, V16-10
starting F2-2, F2-6, F/ApC-6
suspending F2-4, V11-119
use with X-windows F2-1
user interface F2-8, F/ApC-7, O16-8, R1-18
Workstation
Edit Functions R1-13
workstations F2-4
active window F2-6, R1-13
configuring X–Windows F2-4, R1-12
mouse configuration F2-5, R1-12
obtaining help F2-36, R1-8
window accelerators F2-6, R1-13
window buttons F2-5, R1-13
window operations F2-5, R1-12
XC3000 Demonstration Board H1-11
xdm.pro file R1-33, R1-38
XNFMAP R2-44
X–Windows F2-6, R1-14
xdm.pro file F2-2, R1-9, R1-34, R1-38, V7-11, V7-12, V11-115
displaying contents of F2-40
reading F2-40
saving options in R1-33
writing F2-40
XDraft program O11-6
accessing through XDM R1-23
error messages O/ApB-1
options O2-8, O/ApA-1
SDT changes O2-9
support O1-4
VST changes O2-11
connectivity database extension O2-11
Vst.cfg file O12-3
warning messages O/ApC-1
XDraw V13-15, V14-20
XEMake A1-9, A1-12, A5-8, L1-37, V5-15, V10-1, V10-16, V10-22
accessing through XDM R1-20
assembling equations V5-13
command summary O7-10
default operation V7-13
design flow V1-4, V7-7, V7-8
file formats O7-10
input files O7-10
output files O7-11
flow chart O7-8
initially processing designs V7-13
input V7-10
invoking O7-8, V5-14, V16-33
command line V7-9
XDM V7-8
options O7-10
output V7-11
programs run automatically V7-10, V16-33
purpose V7-1, V7-7
reprocessing designs O7-13, V7-14
XEPLD A7-1
adding bus in ViewDraw V16-19
adding bus label to schematic in ViewDraw V16-24
adding labels to schematic in ViewDraw V16-22
adding nets in ViewDraw V16-20
assigning attributes in ViewDraw V16-25
assigning signals to pins V16-27
changing project directory V16-46
changing sheet size in ViewDraw V16-15
checking the design V16-32

XEPLD *(Continued)*
- command summary O/ApD-1
- configuring environment V16-10
- creating Boolean equations V16-29
- creating custom symbol V16-47
- creating lower-level schematic V16-52
- creating new schematic in ViewDraw V16-11, V16-15
- creating programming file V16-37
- declaration statements V16-29
- defining PLD equations V16-29
- devices F2-17
- entering ViewDraw schematic components V16-16
- exiting Workview V16-28, V16-54
- finishing schematics in ViewDraw V16-26
- fitter A7-4, A7-5, V16-22, V16-23, V16-32, V16-33, V16-34, V16-35, V16-37
- fitting the design V16-32
- functional simulation
  - PLD symbols V16-28
  - preparation V16-54
  - running V16-54
- functional simulation *see also* functional simulation
- including xact software in path V16-5
- installing V16-5
- installing Workview library V16-5
- invoking fitter V16-34
- invoking the fitter V16-33
- invoking XDM V16-6
- overview F1-1, F5-1
- placing custom symbol in schematic V16-49
- renaming schematics in DOS V16-28
- reports V16-35
  - assembler log V16-35
  - fitter error V16-35
  - logic optimizer V16-36
  - mapping V16-36
  - partitioner V16-36
  - Pinlist V16-23
  - pinlist V16-36
  - resource V16-35
- saving pin assignments V16-36
- saving schematic in ViewDraw V16-28
- *see also* timing simulation
- setting XACT variable V16-5
- timing simulation
  - command file V16-41
  - displaying back-annotated values V16-44
  - preparation V16-37
  - preparing input vectors V16-39
  - running V16-41
  - viewing results V16-43
- tutorial M16-1
  - .err file M16-38
  - .lga file M16-38
  - .lgc file M16-38
  - .map file M16-38
  - .par file M16-38
  - .pin file M16-38
  - .res file M16-38
  - add bus M16-41
  - add list M16-41
  - add pins M16-46
  - add symbol name M16-49
  - add trace M16-41
  - adding bus names M16-25
  - adding names M16-22
  - adding symbols M16-16
  - assembler log report M16-38
  - assigning signals M16-31
  - attributes M16-28
  - Boolean equations M16-32, M16-33
  - bus command M16-18
  - bus names M16-25
  - bus rippers M16-21, M16-26
  - check symbol M16-49

XEPLD, tutorial *(Continued)*
checking design M16-31
complete UART schematic M16-30
creating a bus M16-18
creating a schematic M16-15
creating wires M16-20
custom symbols M16-45
delete force M16-41
deleting symbols M16-17
demonstration summary M16-7
design architect M16-12
design description M16-5
do file M16-40
draw symbol M16-46
drawing design M16-12
EQUATIONS keyword M16-33
example files M16-6
fitter M16-22, M16-37
fitter error report M16-38
fitting the design M16-37
force command M16-41
global property M16-28
installing M16-1
Intel Hex file M16-37
JEDEC M16-37
lengthen pins M16-48
list file M16-43
logic optimizer report M16-38
mapping report M16-38
open symbol M16-46
PALASM M16-37
partitioner report M16-38
pinlist report M16-38
placing symbol M16-50
PLD equations M16-32
PLD file M16-32
PLD=filename M16-28
PLD_DMGR M16-11
PLD_FNCSIM8 M16-54
PLD_Men2XNF8 M16-37, M16-54
PLD_TIMSIM8 M16-42
PLD_XEMake M16-37
PLD_XEMake reports M16-38
PLUSASM M16-32
preparing system M16-10
properties M16-28
QuickSim II M16-40, M16-54
RCVR.PLD file M16-32
RCVRSUB M16-51
required software M16-1
resource report M16-38
run command M16-42
save symbol M16-49
saving design M16-32
Session 1 M16-10
Session 2 M16-12
Session 3 M16-32
Session 4 M16-37
Session 6 M16-45
session overview M16-9
simulation M16-39, M16-54
symbol window M16-45
trace file M16-44
UART M16-5
UART schematic M16-13
unified library M16-16
viewing design M16-13
wire command M16-20
XACT library M16-16
zoom level M16-15
using Workview labels V16-36
zooming in ViewDraw V16-15
XEPLD.CFG file E5-23, F5-13
XFF file M10-7, R2-32, R2-36, U5-2, V7-6, V7-10, V10-2, V10-4, V10-5, V10-6, V10-11, V10-12, V13-15, V13-19, V14-23, V14-25, V15-24
output by XNFMerge R2-167, R2-168, R2-170, R2-172
XFind V12-31, V13-14, V14-19
Xform menu V/ApA-27
Xform-reflect command V/ApA-28

Xform-rotate command V16-17, V/ApA-27
Xform-scale command V/ApA-28
Xform-stretch command V/ApA-13, V/ApA-29
XFW file V13-15, V14-19
XG file R2-32, V7-6, V10-2, V10-5, V10-6, V10-11, V10-12, V13-22
  output by X-BLOX R2-170, R2-172
XGS file M10-7, M10-29
Xilinx ABEL M3-9, M6-5, M10-3, M10-14, U2-3
  ABEL-HDL file *see* ABEL-HDL file
  ABL2XNF V14-10, V14-19, V14-23
  adding symbol to schematic M3-9
  bus vectors V14-7
  compiling ABEL-HDL file V14-10
  creating a routed design with XMake V14-21
  creating a symbol M3-9
  creating Viewlogic symbol V14-11
  creating Workview project directory V14-2
  definition A1-1
  designs supported A1-12
  documentation A1-13
  EPLD design flow A1-4, A7-1
  examining XSimMake output V14-18, V14-25
  example file O14-6
  exiting A5-9, A6-21, V14-10
  families supported A1-1
  files used A1-5
  flip-flop support A1-11
  FPGA design flow A1-2
  functional simulation V1-3, V6-7, V10-5, V12-28, V12-29, V14-16, V14-17, V14-20
  functional simulation *see also* functional simulation V6-3
  functional simulation with VST O14-16
  help A2-6, A5-2, A6-16, A6-36
  incompletely-specified state machines A1-11
  intermediate files A5-10
  internal simulator O14-10
  invoking V14-4
  invoking from operating system A1-1, A2-1, A5-1
  invoking from XDM A1-1, A2-1, A5-1
  invoking from XMake A1-1
  logic-level specifications A1-10, A9-13
  major features A1-9
  mapping A1-10
  merging files with XNFMerge V7-6, V10-4
  optimization A9-5
  placing symbols in schematics O14-14
  platform availability A1-1
  programs used A1-5
  replacing block with Xilinx ABEL module in ViewDraw V14-12
  saving signals A1-11
  simulation schematics V12-33
  simulation types A1-9
  simulator V14-8, V14-10, V14-21
  state encoding A1-9
  symbol creation O14-11
  symbols V1-3
  synthesizing EPLD state machines A5-6
  test vectors V14-8, V14-9
  timing simulation M8-3, V1-3, V12-49, V14-24, V14-26
  timing simulation *see also* timing simulation V8-2
  tutorial M14-1
    ABL2XNF M14-12
    adding STAT_ABL to calc M14-13
    back-annotation M14-23
    creating a symbol M14-12
    design description M14-3
    do file M14-20, M14-25

Xilinx ABEL, tutorial *(Continued)*
files V14-2
file property M14-14
FNCSIM8 M14-15
functional simulation M14-15
Gen_Sch8 M14-15
Gen_Sym8 M14-12
implementation M14-20
installing M14-2
PLD_FNCSIM8 M14-15, M14-17
PLD_FNCSIM8 output M14-18
PLD_Men2XNF8 M14-16
PLD_Men2XNF8 output M14-16
PLD_TIMSIM8 M14-23
PLD_TIMSIM8 output M14-24
PLD_XMake M14-20
PLD_XMake output M14-22
QuickSim II M14-20, M14-25
required software M14-1
STAT_ABL M14-3, M14-14
synthesizing Xilinx ABEL M14-11
timing simulation M14-23
verifying design with demo board M14-23
verifying STAT_ABL M14-11
viewing schematic M14-18
viewing STAT_ABL.ABL M14-3
XAS file M14-12
Xilinx ABEL output M14-7
XSF file M14-12
unsupported features A1-12
updating designs automatically A1-12
verifying symbol attributes in View-Draw V14-15
verifying symbol type in ViewDraw V14-14
viewdraw.ini file V14-3
viewing schematic in ViewDraw V14-14
XABEL A1-9
XSimMake output (functional) O14-16
XSimMake output (timing) O14-25
Xilinx ABEL design files
merging into OrCAD design files O4-21
Xilinx ABEL elements R1-116
Xilinx attributes
see properties
Xilinx Design Editor , see XDE
Xilinx Design Manager A1-6
see XDM, PLD_XDM
Xilinx FPGA options dialog box A6-8
Xilinx libraries M3-4
Xilinx macros L1-93
Xilinx Netlist Format R1-2, U3-1
Xilinx Property dlc2p keyword A4-4
Xilinx Property dlc2s keyword A4-4
Xilinx Property dlp2p keyword A4-4
Xilinx Property dlp2s keyword A4-4
Xilinx Property-Initialstate statement V14-8
Xilinx Property-Initialstate keyword A3-11, A3-12, A3-13, A3-18, A4-2
Xilinx Property-Map keyword A1-10, A4-3, A4-16, A9-3
Xilinx Property-Save keyword A4-3, A4-16, A9-1
Xilinx Synopsys Interface U2-3
Xilinx Technical Bulletin Board U8-19
Xilinx-EPLD-options dialog box A6-10, A6-26, A7-15, A7-16, A9-37
Xilinx-FPGA-options dialog box A6-24, A9-5
Xilinx-Property-Initialstate keyword A9-20, A9-21, A9-28
XMake A1-1, A1-6, A1-9, A1-12, A4-18, R1-116, R2-227, U3-1, U3-2, U5-1, V10-5, V13-1, V13-11, V14-1, V14-25, V15-2, V15-22
accessing through XDM R1-20
configuring V11-114
config. for incremental design V11-143

XMake *(Continued)*
creating bitstream V11-118, V11-145
creating routed XACT-Performance design V15-23
creating routed X-BLOX design V13-18
creating routed Xilinx ABEL design V14-21
default operation V7-13
design flow V1-4, V7-2, V7-3, V11-1
error messages R1-51
errors V11-120, V11-145
executing XNFPrep R2-29, R2-31, R2-35
HDL file R1-38
initially processing designs V7-13
input V7-10
input file formats
ASCII HDL file R1-37
MAK file R1-37
schematic file R1-37
top-level XNF file R1-37
inputs
MAK files R1-38, R1-46
schematic drawing files R1-38
XNF files R1-38
invoking
command line V7-4
XDM V7-4
invoking ABL2XNF A5-7
MAK file M7-3
MAK file input R1-42
MAP file R1-39
optimized XNF file R1-39
options V7-5
creating XFT file R1-41
directing output to screen R1-41
disabling MakeBits R1-41
displaying explanations R1-42
flattening design R1-42
generating abbreviated MAK file R1-40
generating X-BLOX MAK file R1-40
-l V7-5
mapping macro logic R1-39
-p V7-5
-r V7-5
reprocessing design R1-41
setting part type R1-41
translating design to LCA file R1-42
-x V/ApD-2
OUT file R1-38
outputs V7-11, V11-12, V11-119, V13-19, V14-22, V15-23
BIT files R1-39
LCA files R1-39
MAK files R1-38, R1-46
partitioned XNF file R1-39
programs run automatically V7-6, V10-1
purpose R1-3, V7-1, V7-2, V11-114
reprocessing designs V7-14
running ABL2XNF V14-23
running APR V14-23
running MakeBits V14-23
running PPR R2-187, V13-20, V14-23
running WIR2XNF V13-19, V14-23
running X-BLOX V13-20
running XDelay V13-20, V14-23
running XNFMAP V13-20, V14-23
running XNFMerge V13-19, V14-23, V15-14
running XNFPrep V13-20, V14-23
schematic file input R1-42
script file V11-12
stop-to-review-DRC option V13-20
trimmed, flattened XNF file R1-39
warnings V11-120
XFF file R1-39
XG file R1-39
XNF file R1-39

XMAKE menu
command E4-4, E4-8
XMake program B3-10, O7-2
command summary O7-6
configuring for incremental design O11-98
file formats
input files O7-10
output files O7-11
flow chart O7-3
invoking O7-4
options O7-7
output files O11-74
reprocessing after changes O7-13
XMD
Verify menu
VSMUPD R1-27
XMM file V6-11
XNF file E5-3, E5-4, L1-13, L1-55, L1-57, L1-58, L1-64, L1-67, L1-69, L1-70, M6-1, M6-5, M7-1, M10-7, O4-21, O4-22, R2-167, R2-168, R2-170, R2-172, R2-185, V10-18
BAX R3-48
block-only information R3-30
compiling with SynthX A1-1, A1-6, A1-8, A5-5
converting to different versions R1-108
corrupt R2-18
corrupted V/ApE-5, V/ApE-6, V/ApE-7, V/ApE-8, V/ApE-9
created by StateX A1-6
creating V10-2
creating from ABL file A5-7, A6-7, A6-33
delay information R3-31
design verification R1-3
electrical rule check V11-1
excluding delay information R3-32
FILE attribute V1-4, V3-10, V4-3, V6-8, V14-15, V14-21
files
merging F2-23
RPM B6-2
gate-only information R3-31
hierarchical signal names V3-2
hierarchy in R2-11
including third-party designs V3-9, V7-6, V10-2, V10-4, V14-23
incorporating into schematic A1-7, A5-9
input to FITNET V7-1
input to VSMUPD V10-20, V10-22, V/ApD-4
input to XNF2WIR V8-3, V10-12, V10-15, V10-16, V10-17, V14-19, V16-38
input to XNFMerge V7-6, V7-10, V10-2, V10-4, V10-6, V11-148, V13-19, V14-20, V16-33
input to XNFPrep R2-29, R2-32, R2-34
LCA2XNF R1-5, R3-30
loadless/sourceless nets R3-33
logic optimization with ImproveX A1-6
MemGen R1-60
merging V7-6, V7-10, V10-2, V10-4, V10-6, V11-1, V11-148, V13-19, V14-20, V14-23, V16-33
output by ABL2XNF V6-10, V11-10, V11-11, V14-11, V14-14, V14-16, V14-23
output by LCA2XNF V7-1, V10-11, V10-14, V12-58, V13-22, V14-25
output by MemGen V4-15, V6-11
output by VMH2XNF V8-3, V10-16, V10-22, V10-23, V16-38, V/ApD-5
output by WIR2XNF V7-6, V7-10, V10-3, V10-23, V11-11, V11-148, V13-14, V13-19, V14-19, V14-23, V16-33, V/ApD-2, V/ApD-3, V/ApD-17, V/ApD-18, V/ApE-3

XNF file *(Continued)*
output by X-BLOX V13-15
output by XEMake V7-7, V7-13
output by XMake V7-2, V7-13, V11-1
output by XNFBA V10-11, V10-15, V10-20, V13-22, V14-25
output of HM2RPM R1-113, R1-117
output of XNFPrep R2-34, R2-36
pin names A9-1
primitives A6-43
purpose V7-1
referenced by symbols V12-29, V12-32, V12-33, V12-49
routed V9-2, V10-11, V10-15, V10-20, V10-21, V10-22, V/ApD-4
running BLIFOPTX before SynthX A6-9, A6-25
saving pin names A1-11
signal binding R2-6
specifying output directory A6-40, A6-43
specifying output file name A6-40, A6-43
symbols A6-10, A6-26, A6-40, A6-43, R2-6
translation U3-3
translation to VSM file V10-5, V10-6
TSPEC symbols A1-10
types V10-2, V10-6, V10-12
unified libraries symbols V7-5
unrouted V10-20
versions R1-105, R1-106
X-BLOX modules V4-17
XNFBA R1-5
XNFCvt R1-106
XNFMAP R1-4
XNFMerge R1-4, R2-1, R2-2, R2-3, R2-6
xnf subdirectory V6-8, V10-23, V16-33
XNF2INF program O10-19
XNF2VST
accessing through XDM R1-28
command F2-29
program O1-3, O10-16, O10-18
enhancements O1-5
error messages O/ApB-5
program options O/ApA-2
signal names O10-22
syntax O10-19
timing simulation
syntax O10-16
warning messages O/ApC-4
XNF2WIR A7-19, A7-20, V10-17, V12-2
accessing through XDM R1-29
command F2-21
error messages V/ApE-5
inputs V10-18, V/ApE-4, V/ApE-9
invoking
command line V10-8, V10-10, V10-12, V10-15, V10-16, V10-18, V16-39
XDM V10-17
options
-a V/ApD-1
-b V/ApD-1
-c V/ApD-1
-l V/ApD-2
-m V16-38, V/ApD-2
-s V9-5, V/ApD-2
-x V9-5, V/ApD-2
outputs V10-8, V10-10, V10-18, V13-15, V14-20, V14-26
placing library aliases in WIR file V/ApD-2
placing OSC attributes in WIR file V/ApD-2
purpose V10-5, V10-8, V10-10, V10-12, V10-15, V10-17
returning net names to original format V/ApD-2
running with XSimMake V8-3, V13-15, V14-19, V14-25, V16-38

XNF2WIR *(Continued)*
setting maximum symbol number in WIR file V/ApD-2
specifying AKA file name V/ApD-1
specifying CRS file name V/ApD-1
suppressing output messages V/ApD-1
warning messages V6-8, V/ApE-1
XNFBA M10-15, M10-17, V10-11, V10-15, V10-17, V10-20, V10-21, V13-22, V14-25
accessing through XDM R1-28
error messages M/Ap-10
purpose R1-5
Syntax M10-31
variables M10-31
XNFBA program
timing simulation
syntax O10-16
XNFCVT
accessing thorugh XDM R1-28
AKA file R1-106, R1-108
conversion process R1-108
error messages R1-109
inputs R1-106
name prefixes R1-108
options R1-106
excluding AKA file R1-106
specifying XNF file version R1-106
outputs R1-106
purpose R1-4, R1-105
syntax R1-105
XNF file differences R1-106
XNF target file version R1-106
XNFDRC R2-227, R2-239
invoking from XDE R3-61, R3-125
turning automatic checking on/off R3-98
XNFMAP L1-35, L1-47, L1-49, L1-61, U3-2, U5-2, V4-10, V7-6, V10-10, V10-11, V10-15, V11-12, V11-144, V13-20, V14-23, V/ApE-1
-a option R2-45
accessing through XDM R1-23
AKA file R2-55
BLKNM parameter R2-61
-c option R2-45
CLB mapping R2-50
CLBMAP symbols R2-43, R2-57
closed R2-58
locked pins R2-58
MAP parameters R2-58
open R2-58
unlocked pins R2-58
XC3000 design R2-59
command–line syntax R2-44
controlling partitioning R2-61
CRF file R2-43, R2-45, R2-50, R2-56, R2-67
sample output R2-68
-e option R2-46
error messages R2-82
explicit (X) attributes R2-60
-f option R2-46
FILE= attribute R2-48
-g option R2-46
guided design R2-47, R2-177
AKA file R2-55
CLBMAP symbols R2-53
LCA file R2-54
output R2-53
PBK file R2-53
PGF file R2-53
HBLKNM parameter R2-61, R2-62
-i option R2-46
input files R2-44, R2-49
PGF file R2-44
XTF file R2-44
introduction R2-43
-j option R2-47
-k option R2-47, R2-55
LCA file R2-54
LOC parameters R2-61, R2-62, R2-63

XNFMAP *(Continued)*
logic mapping R2-50
logic placement R2-62
IOBs R2-64
multiple–block LOC R2-63
pull-ups R2-65
single–block CLB R2-63
TBUFs R2-64
-m option R2-47
MAP file R2-43, R2-44, R2-50
for MAP2LCA and APR R2-69
for PPR R2-71
output R2-72
maximize signal sharing within CLBs R2-46
-n option R2-47
-o option R2-47
options R2-45
change LCA part type R2-48
ease requirements for combining logic R2-45
estimate LCA resources R2-46
force dense partitioning of logic R2-46
guide previous design iteration R2-47
ignore CLBMAP symbols R2-47
ignore IO location constraints R2-47
ignore location constraints R2-47
limit gates in CLB R2-46
-k R2-177
-m R2-184
-p R2-48
reduce number of CLBs R2-48
relax signal–combining requirements R2-49
respect guide file hierarchy R2-49
respect hierarchy boundaries R2-45
suppress registered signal ordering R2-47
use direct flip–flop input pins R2-46
output files R2-44, R2-50, R2-65
CRF file R2-45, R2-67
MAP file R2-44, R2-69, R2-71
PBK file R2-45
outputs R2-66, R2-165
pairing flip–flops R2-50
partitioning flip–flops R2-50
partitioning gates into function generators R2-165
partitioning guide file R2-52
partitioning logic on schematic R2-57
PBK file R2-45
PGF file R2-43, R2-44, R2-45, R2-47, R2-50, R2-52, R2-56
processing R2-49
purpose R1-4
-q option R2-48
-r option R2-48
register ordering R2-50
naming conventions R2-51
OrCAD/SDT R2-51
respect macro boundaries R2-48
-s option R2-49
swapping CLB pins R2-58
syntax R2-44
-u option R2-49
use with XDM R2-44
warning messages R2-73
XC3000A/L PPR design flow R2-168
XC3000A/L PPR design flow with X-BLOX R2-172
XTF file R2-44
XNFMerge L1-14, L1-15, L1-17, L1-19, L1-76, L1-77, L1-81, L1-82, L1-85, L1-86, L1-91, L1-93, L1-94, M10-5, M10-7, M10-11, M10-15, R2-176, U3-2, U5-2, U5-3, V10-6, V10-8, V11-11, V16-33
accessing through XDM R1-23

XNFMerge *(Continued)*
- binding by signal name R2-7
- binding signals between levels R2-6
- binding symbols by pin name R2-8
- command F2-23
- error messages R2-17
- FILE attribute V4-3
- flattened files R2-1
- hierarchical files R2-1
- inputs
  - MAP file R2-3
  - XNF file R2-3
- location parameter propagation R2-10
- lower-level files R2-1
- non–primitive symbols R2-5
- options R2-4, V10-4
  - abbreviating messages R2-4
  - accepting unknown symbols into design R2-5
  - changing merge report file name R2-5
  - searching directory for XNF/MAP files R2-4
  - specifying LCA device type R2-5
- outputs V10-5
  - MRG file R2-3
  - XNF file R2-3
- primitive symbols R2-5
- processing hard macros R1-111, R1-112, R1-113, R1-114, R1-116, R1-118
- program description M10-34
- purpose R1-4, V10-4
- renaming signals and symbols R2-9
- report file V11-11
- running with XEMake V7-7, V7-10
- running with XMake V7-2, V7-6, V13-19, V14-23, V15-14
- running with XSimMake V13-15, V14-20
- searching for MAP and XNF files R2-6
- signal binding R2-2
- symbol resolution R2-2
- syntax R2-2, V10-4
- TIMEGRP errors V15-8
- TNM attribute V4-9
- top-level files R2-1
- tutorial design files M11-10
- USE_RLOC constraint V4-6
- warning messages R2-14
- XC3000A/L PPR design flow R2-168
- XC3000A/L PPR design flow with X-BLOX R2-172
- XC4000 PPR design flow R2-167
- XC4000 PPR design flow with X-BLOX R2-170

XNFPrep L1-20, L1-100, L1-101, M7-8, M10-7, M10-11, M10-29, U3-2, U5-2, U5-3, U5-5, V4-10, V7-6, V10-5, V10-6, V10-9, V10-10, V11-11, V11-116, V11-119, V11-120, V11-121, V13-15, V13-20, V14-23, V15-8, V15-24
- accessing through XDM R1-23
- CY4 symbols R2-42
- design flow R2-29
  - XC2000 R2-32
  - XC2000L R2-32
  - XC3000 R2-32
  - XC3100 R2-32
- design flow with X-BLOX
  - XC3000A R2-31
  - XC3000L R2-31
  - XC3100A R2-31
  - XC4000 R2-31
- design flow without X-BLOX
  - XC3000A R2-30
  - XC3000L R2-30
  - XC3100A R2-30
  - XC4000 R2-30
- examples of use R2-37
- families supported R2-29
- ignoring LOC constraints R2-35, R2-38

XNFPrep *(Continued)*
ignoring RLOC constraints R2-35, R2-38
ignoring XACT-Performance parameters R2-36, R2-39
inputs
XFF file R2-32
XG file R2-32
invoking
command line R2-34
XDM R2-34
loadless signals R2-42
log file R2-33, R2-39
obtaining help R2-35, R2-38
options
cstfile R2-36, R2-37
helpall R2-35, R2-38
ignore_rlocs R2-35, R2-38
ignore_timespec R2-36, R2-39
ignore_xnf_locs R2-35, R2-38
logfile R2-33, R2-39
outfile R2-33, R2-36, R2-40
paramfile R2-40
parttype R2-36, R2-41
report R2-32, R2-36, R2-41
savesig R2-35, R2-41, R2-190
outputs R2-165
PRP file R2-32, R2-41
PRX file R2-32, R2-41
XTF file R2-33, R2-40
XTG file R2-33, R2-40
processing hard macros R1-114, R1-116
program description M10-35
purpose R1-4, R2-29
renaming log file R2-33, R2-39
running in XMake R2-35
sourceless signals R2-42
specifying options in parameter file R2-40
specifying output file name R2-36, R2-40
specifying part type R2-36, R2-41
specifying report file name R2-36, R2-41
submitting constraints file R2-36, R2-37
trimming hard macro default logic R1-112
trimming signals R2-35, R2-41
X-BLOX design flow R2-29
XC2000 design flow R2-32
XC2000L design flow R2-32
XC3000 design flow R2-32
XC3000A design flow with X-BLOX R2-31
XC3000A design flow without X-BLOX R2-30
XC3000A/L PPR design flow R2-168
XC3000A/L PPR design flow with X-BLOX R2-172
XC3000L design flow with X-BLOX R2-31
XC3000L design flow without X-BLOX R2-30
XC3100 design flow R2-32
XC3100A design flow with X-BLOX R2-31
XC3100A design flow without X-BLOX R2-30
XC4000 design flow with X-BLOX R2-31
XC4000 design flow without X-BLOX R2-30
XC4000 PPR design flow R2-167
XC4000 PPR design flow with X-BLOX R2-170
xnfprep.log file R2-33, R2-39
XOR attribute A7-14
XOR gates A7-1, A7-2, A7-16
XOR_factors directive A7-16
XOR7 L1-33, V5-11, V5-21
XOR8 L1-33, V5-11, V5-21
XOR9 L1-33, V5-11, V5-21

XORBUS module B4-2, B4-6
XORBUS1 module B4-2
XORBUS2 module B4-2, B4-6, B4-7
XORBUS2 symbol V13-10
XPP(Xilinx PROM Programmer) H4-1
accessing through XDM R1-29
command-line parameters
-dev name H4-19
-help H4-19
-setup H4-19
commands H4-19
append H4-21
check H4-20
checksum H4-20
compare H4-20
copy H4-20
numdev H4-18
program H4-19
read H4-21
setup H4-21
configuring settings H4-5
baud rate H4-6
device count H4-6
device name H4-6
port name H4-6
sound H4-6
environmental variables H4-5
MACHINE H4-5
PATH H4-5
XACT H4-5
error messages H4-27
examples H4-22
interactive commands H4-24
append H4-25
baud H4-24
check H4-25
compare H4-25
copy H4-25
count H4-24
design H4-24
device H4-24
help H4-24
path dir H4-25
port H4-25
program H4-26
read H4-25
reset H4-25
setup H4-25
sound H4-25
interactive mode H4-23
syntax H4-24
programming flow H4-1
searching a design file H4-26
setup H4-3
using on PCs H4-7
batch mode H4-17
function keys H4-8
interactive mode H4-9
adding data to programmed device H4-15
calculating device checksum H4-13
changing profile H4-16
checking if PROM is blank H4-13
comparing programmed device to file H4-13
creating batch file H4-16
programming device from existing device H4-12
programming device from file H4-10
reading device and creating file H4-14
options
changing configuration information H4-8
displaying help H4-8
executing batch file H4-8
setting device type H4-8
setting RESET line polarity H4-8

XPP, using on PCs, options *(Continued)*
specifying LCA file H4-8
using ANSI video H4-7
syntax H4-7
using on workstations H4-18
syntax H4-18
xpp.pro file H4-18
XPP Profile
xpp.pro H4-17, H4-26
XRP file V15-39, V15-40, V15-42
XSF file A1-6, A1-7, A1-8, A1-13, A5-5, A5-7, A5-9, A5-10, M3-9, V6-10, V14-10, V14-11
EPLD M5-14
XSI U2-3
XSimMake A1-8, A1-9, A1-12, A7-18, R1-116
accessing through XDM R1-28
command F2-28
creating simulation directories V6-2, V8-2, V12-29, V13-12, V14-17
design flow V1-4, V6-4, V8-2, V8-3, V8-4, V12-2
designs with CLB/IOB primitives V6-11
designs with FILE attributes V6-3, V6-8
designs with hard macros V6-8
designs with MemGen components V6-3, V6-11, V8-2, V12-29, V12-49
designs with special symbols V1-4, V6-1, V6-3, V8-1, V8-3, V12-31, V12-33
designs with X-BLOX modules V6-3, V6-8, V6-10, V8-2, V12-28, V12-29, V12-49, V13-11
designs with Xilinx ABEL components V6-3, V6-10, V8-2, V12-28, V12-29, V12-49, V14-15
designs without special symbols V6-2, V8-2, V12-29, V12-30
directory structure V6-2
EPLDs V6-7, V8-3, V16-37
flow types V6-6
generating functional simulation netlist V6-1, V6-2, V12-1, V12-28, V12-30, V14-16, V14-17
generating timing simulation netlist V1-4, V8-1, V8-2, V12-1, V12-48, V12-49, V13-21, V14-24, V16-37
input V6-3, V8-2
invoking V6-5
command line V8-5
XDM V8-4
menu E5-4
options
-f V6-6
-h V6-6
-l V6-6
-o V6-6
-p V6-6
-r V6-7
-v V6-7
output V6-3, V6-7, V8-2, V12-31, V12-50, V13-14, V13-22, V14-18, V14-25
program
functional simulation O6-2
command summary O6-4
FPGA designs O12-10
options O6-3
subprograms O6-4
syntax O6-2
output files O12-14
timing simulation
command summary, EPLD O8-5
command summary, FPGA O8-5
EPLD devices O8-5
FPGA devices O8-5
options O8-3
syntax O8-2

XSimMake *(Continued)*
programs run automatically V10-1, V14-19
purpose V1-3, V12-1
running ABL2XNF V14-19
running Check program V13-14, V13-15, V14-19, V14-20
running LCA2XNF V13-22, V14-25
running VMH2XNF V8-3, V16-38
running VSM V8-4, V13-16, V14-20, V14-26, V16-38
running VSMUPD V13-23, V14-26
running WIR2XNF V13-14, V14-19
running XDelay V13-22, V14-25
running XDraw V13-15, V14-20
running XFind V12-31, V13-14, V14-19
running XNF2WIR V8-3, V13-15, V14-19, V14-25, V16-38
running XNFBA V13-22, V14-25
running XNFMerge V14-20
syntax V6-5
Xterm option A6-32
X–terminal windows F2-5, R1-12
XTF file L1-55, L1-57, L1-64, L1-67, L1-69, L1-70, M10-7, M10-29, R2-33, R2-40, R2-44, V7-6, V10-2, V10-5, V10-10, V10-12, V13-20
input to PPR R2-165, R2-174
output by XNFPrep R2-167, R2-168, R2-170, R2-172, R2-174
partitioning into function generators R2-165
XTG file R2-33, R2-40, V7-6, V10-5, V10-9, V13-20
output by XNFPrep R2-170, R2-172
XTM file V15-29
X-value 0 option A6-14
X-value 1 option A6-14
X–Windows
in XDM F2-1, F2-4

## Z

Z option A6-49
ZIF socket
XPP H4-17
zoom
commands O11-45, O16-13
Z-value 0 option A6-14
Z-value 1 option A6-14